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Optimized (2nd Pass) Gallium Arsenide (GaAs) Integrated Circuit Radio Frequency (RF) Booster Designs for 425 MHz and Dual Band (425 and 900 MHz)

by John Penn

ARL-TR-5396 **November 2010**

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John Penn
Sensors and Electron Devices Directorate, ARL

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14. ABSTRACT

High-performance microwave and radio frequency integrated circuits are of interest to the Army. Several monolithic microwave integrated circuits (MMICs) were designed to enhance the performance of commercial-off-the-shelf (COTS) RF integrated circuits (RFICs) used in many wireless systems. This report documents a set of MMIC designs optimized for the 400 to 450 MHz ultra-high frequency (UHF) band and a dual band design that also includes 850 to 950 MHz operation. Additional incorporation of discrete matching elements into a single integrated IC will improve size and weight of wireless systems. This is an optimized set of designs based on a previous 1st pass design effort. Ten separate MMIC designs were designed and fabricated.

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1. Introduction

Increased transmission range in low-power radio frequency (RF) applications is a common desire within the Army. The RF integrated circuit (RFIC) booster chip is intended to increase range between RF nodes for low-power wireless applications. The booster concept uses the high RF performance advantages of the gallium arsenide (GaAs) process to enhance the capabilities of systems using commercial RFIC transceivers. It can be inserted easily into systems to increase transmit power, receiver sensitivity, and efficiency or battery utilization. In this 2nd pass optimized booster design, lessons learned from a 1st pass design were used to optimize a design for a targeted system performance and battery voltage.

2. Lessons Learned from 1st Pass Design

The first booster chip integrated circuit (IC) consisted of RF circuits to enhance the performance of commercial RFIC transceiver circuits, which could be used in a variety of applications. Of particular interest was a wireless tag at ultra-high frequency (UHF) frequencies using a commercial RFIC transceiver. Lower UHF frequencies tend to propagate further in urban or canopy/forest environments, while higher frequencies provide advantages of smaller antennas and typically higher data rates. Since the multi-project low-cost prototype service provided by TriQuint Semiconductor allows one to customize a 5x10 mm quarter tile into multiple IC designs, many variations of an RF front-end booster design were fabricated for the 1st pass at frequencies of interest at 450, 900, and 2400 MHz with other circuit design variations. This is often called the “shotgun” approach by testing multiple design variations.

Due to the high performance of TriQuint’s 0.5 µm TQPED pseudomorphic high electron mobility transistor (PHEMT) process, low-cost prototyping service, high reliability process, quality control, excellent reputation, and available design models for Agilent’s Advanced Design System (ADS) and Applied Wave Research’s (AWR) Microwave Office (MWO), the TQPED process was used for the 1st pass and 2nd pass booster IC designs. While the 1st pass designs tried a number of circuits at different frequencies, the 2nd pass designs were mostly targeted at operation between 400 to 450 MHz, so one obvious change was to retune the original circuit designs from a center frequency of 450 MHz to the slightly lower 425 MHz. Another design variation targeted a dual band operation around 425 or 900 MHz.

A broadband power amplifier design in the 1st pass was very efficient (~50% power added efficiency [PAE]), had good gain, and had a good output power of 50 mW (17 dBm) with a 3.6-V battery supply. While a 3.6-V supply is a good choice when using a lithium ion rechargeable battery, nominally 3.9 V with regulation to 3.6 V, another popular battery is a non-

rechargeable 3.0-V battery, such as a small coin cell, which can be regulated to 2.7 or 2.8 V. A current mirror bias of the broadband power amplifier allowed good gain over a large supply voltage variation of 2.0 to 5.0 V with good efficiency, while the output power and DC power consumption varies proportionally with the supply voltage. There is a concern that the current mirror bias may slightly reduce the efficiency of the power amplifier over the simple but less robust resistor divider DC bias. Unfortunately, there were not enough data and design variations in the 1st pass to isolate an optimal DC bias choice between these two approaches relative to efficiency. While the 1st pass broadband amplifier design was a good robust stable design, the 2nd pass goal was to design an amplifier to have 50 or 100 mW of power (17, 20 dBm) optimized for a 2.8-V supply voltage. The power amplifiers in the 2nd pass designs were targeted for a narrowband 50-mW design at 2.8 V, a 100-mW design at 2.8 V, and an optimized variation of the 1st pass broadband design that would provide 50 mW for a 3.6-V supply yet would also operate with a 2.8-V supply at a lower output power but good efficiency.

There were two main variations of a low noise amplifier design in the 1st pass. One was a broadband low noise design with moderate gain but consumed about 16 mA of bias current compared to a narrowband approach with about 5 dB less gain that consumed a mere 3 mA of bias current. The low noise amplifiers in the 2nd pass designs were targeted for an ~2-dB noise figure with a narrowband 425-MHz design with 12-dB gain at 3 mA of current consumption and a second broadband amplifier modified from the 1st pass for 425 and 900 MHz operation with 15-dB gain at a moderate current bias of 8 to 10 mA. Unlike the power amplifiers whose efficiencies peak for a particular supply voltage, the performance of both low noise amplifiers varies little over a supply voltage of 2.0 to 5.0 V. The broadband low noise amplifier was used in a dual band 425- and 900-MHz booster IC design, while the narrowband low noise amplifier was used for the 425-MHz booster IC designs.

The positive voltage controlled binary phase shift key (BPSK) modulator from the 1st pass design was reused for the 2nd pass booster IC designs. A minor change was made to retune the filters in the narrowband switched design from a center frequency of 450 to 425 MHz to better suit a desired frequency of operation from 400 to 450 MHz.

The transmit/receive (TR) switch from the 1st pass design had more insertion loss than desired and was modified slightly to improve its operation at the slightly lower UHF frequency around 425 MHz. One reason for the higher than expected insertion loss in the original design was due to too much use of the higher loss metal0 layer for interconnects. The original simulations defaulted to use a single thick metal for all metal types, which did not correctly simulate the higher loss of the thin metal0 layer. While the thin metal0 layer is required for connecting the circuits, the 2nd pass TR switch redesign minimized the use of metal0 and transitioned to the lower loss thick metal1 or thick metal2 layers for less interconnect loss. Also, the PHEMT switches in the TR switch used negative depletion mode PHEMTs in order to handle the relatively high 100-mW power level from the power amplifier. While it would be easier to design a positive voltage controlled TR switch by replacing the depletion mode PHEMTs with

the enhancement mode PHEMTs, this swap only makes sense for the switches in the BPSK modulator circuit where the power handling requirements are much lower. To use positive control voltages for the TR switch with depletion mode PHEMTs requires several large capacitors and a positive reference voltage input. The capacitors need to be large enough to minimize the insertion loss at the lower 425-MHz operating frequency but small enough to fit in the available circuit size. Insertion loss for the 2nd pass TR switch is expected to achieve the 0.5-dB goal over a broad frequency range above 400 MHz, with approximately 0.25 dB of loss due to the PHEMT switches and 0.25 dB of loss due to the tradeoff of capacitor size.

One of the design variations (ARL08M450) from the 1st pass consisting of a BPSK modulator and power amplifier at 450 MHz and positive voltage control was integrated into an existing tag by a system integrator. Unfortunately, testing was still incomplete by the fabrication date for the 2nd pass designs. The status of the system level test is that data appears to be modulating OK, but the output power level is much lower than expected (~10 dB). It is not clear if there is a board problem, a software problem such as an incorrect drive level programmed into the RFIC, a matching problem at the input or output of the booster IC on the system board, or something else. Testing of this particular design was successful at the die level and the board level. The initial tests from a single tag that includes this booster IC do not correlate with previous tests of the design.

Since wire bond parasitics were not significant in the 1st pass designs at the lower UHF frequencies, they were not used for "tweaking" the 2nd pass designs for optimizing performance. Wire bond diagrams for all the designs in a 4x4 mm quad flat no lead (QFN) packages were created before sending the designs out to fabrication to verify the suitability of the input/output/DC pad layouts. Simulations of the overall designs including the TR switch were performed to verify amplifier performance in the top level designs as well as the individual performance as a standalone amplifier.

3. Component Designs and Simulation Results

The power amplifier for the 2nd pass designs were to be optimized for efficiency and a center frequency of 425 MHz, slightly retuned from the 450 MHz of the 1st pass designs. Also, the power output goals were 50 and 100 mW at 2.8 V, which exceed the original 1st pass design. Secondary goals were amplifiers of similar performance for 3.6-V operation. The original power amplifier was a stable broadband design, but a narrowband design optimized for the lower 2.8-V supply voltage with good output power was desired for the 2nd pass design.

An initial reanalysis of the 1st pass power amplifier was performed to look for ways to optimize the efficiency. There was a slight cost in efficiency with the feedback design due to 1 mA of current through a stabilizing resistor on the gate/input of the PHEMT. For the current mirror

bias, a small 5-µm PHEMT was used for a current reference. This was the smallest device size allowed by the ADS TriQuint library for simulation, but the foundry rules allow devices as small as 2 µm. A change in the current reference from 5 to 2 µm would reduce its current consumption from 1 to 0.4 mA. Reducing the parasitic DC current consumption of the current mirror bias and the stabilizing resistor should slightly improve the efficiency of the amplifier relative to the nominal 30-mA DC consumption of the 6- x 80-µm PHEMT of the amplifier.

There was a workaround to force the simulations to work with the small 2-µm PHEMT device, which had to be laid out manually using the Integrated Circuit Editor (ICED) computer-aided design (CAD) program. A similar current mirror circuit was designed by the author, and then fabricated, and tested as part of the Johns Hopkins University Monolithic Microwave Integrated Circuit (MMIC) Design Course in fall 2009. The simulations showed a minimal 0.4 mA of bias used by the current mirror. Unfortunately, there is the possibility that the power amplifier efficiency may be lower due to using the current mirror bias rather than the resistor divider bias. Reducing the DC 1-mA current in the stabilizing resistor requires a large capacitor to block the DC current while maintaining a low impedance RF connection. The cost is the area needed by the capacitor with minimal impact on the RF performance in order to increase the efficiency a few percent.

The first few designs in the 1st pass used negative control voltages for the depletion mode (dmode) PHEMT switches. Later, variations of the first designs were created using positive control voltages to drive enhancement mode (emode) PHEMT switches that replaced the dmode PHEMT switches. Figure 1 shows a plot of the paired designs ARL02M450 and ARL08M450, which consist of a BPSK modulator and a power amplifier for the 450-MHz band. The subtle differences between the two designs are the positive emode switches in the BPSK modulator of ARL08M450 and the current mirror robust DC bias in ARL08M450 versus a simple resistor divider gate bias in ARL02M450. The performance of the nearly identical second design was slightly less than the original design. Simulations along with measurements of some test circuits indicated that the emode PHEMT switches in the second design should not compress at the signal levels at the input of the modulator. This would seem to indicate that the lower performance was partly due to the current mirror. The output power and efficiency of the original resistor gate bias approached 50 mW and 50% PAE, while the current mirror bias peaked near 40 mW with less than 40% PAE. Figure 2 shows a plot of output power in mW (blue), PAE in percent (green), and gain in dB (red) versus current IDS in mA. Normally, performance plots are shown versus the input power but these were plotted versus current bias. Note that the resistor bias design (ARL02) acts like a typical Class AB amplifier, where the DC bias increases with increasing input power and similarly increased output power. The current mirror bias seems to saturate, limiting the output power and efficiency. However, note that the current range is narrower for the current mirror design. It is performing its expected function of biasing the amplifier at a controlled current. Tables 1 and 2 summarize the performance measurements for the two designs in a spreadsheet format. Some of the lower efficiency of the 2nd design can be

explained by the additional parasitic 1-mA current mirror, which will be reduced to 0.4 mA in the 2nd pass designs. Additional simulations of the amplifier using the current mirror bias were performed using TriQuint's TOM3 model as well as the more advanced TOM4 model but gave no indication of a performance difference between a current mirror bias relative to a resistor divider gate bias. Given this unknown, the 2nd pass power amplifiers use the current mirror bias, but have a test pad connected through a large resistor to monitor the DC gate bias voltage, as well as providing a means to override the current mirror bias. One goal in testing the power amplifiers in the 2nd pass will be to determine which DC bias scheme provides the more efficient amplifier performance.

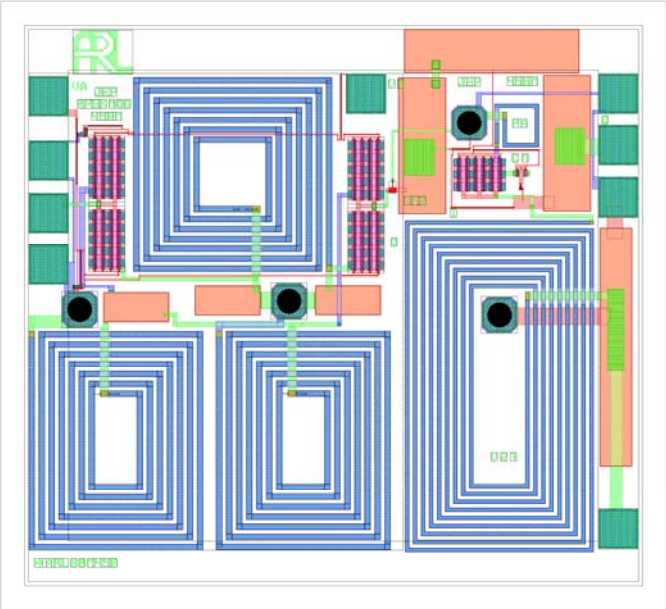

Figure 1. Layout of 1st pass ARL08M450—BPSK modulator and power amplifier.

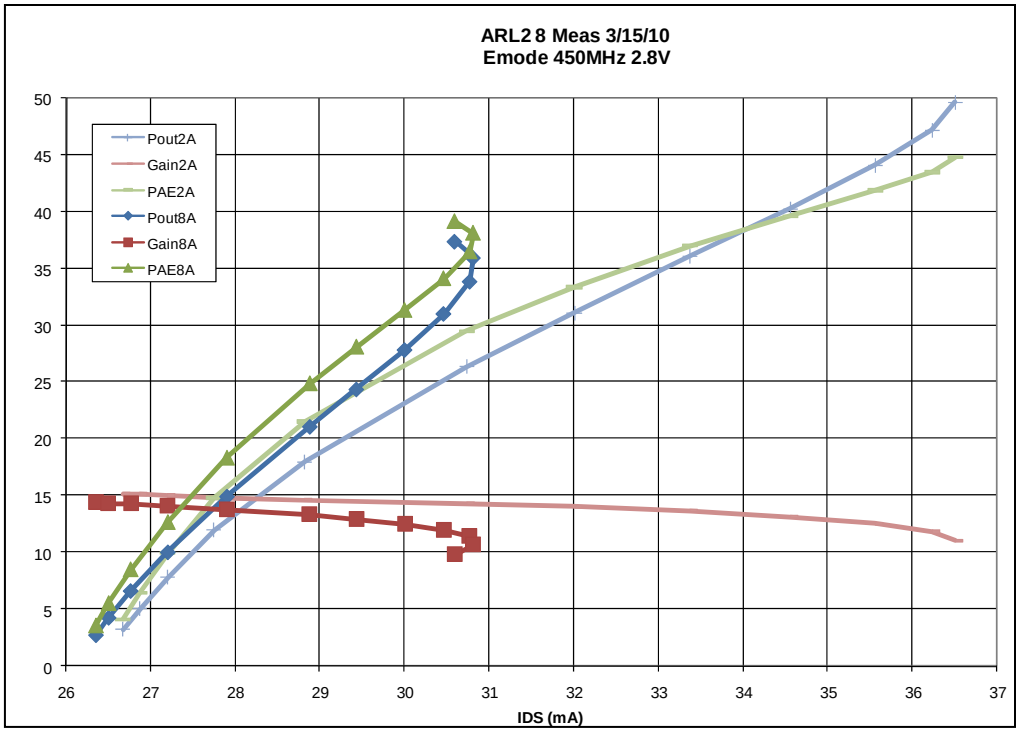

Figure 2. Comparison of performance of 1st pass ARL02M450 vs. ARL08M450.

Table 1. Measured power performance of 1st pass ARL02M450.

BPSK + Power Amps--450 MHz at 2.8 V					0.20 - 0.25 dB loss on DUT QFN3x3 Thru 400-500M Meas				
New Boards measured at 450 MHz		3/15/2010							
450 MHz	PKG#2A	**PA450MHz Emode ARL #8 Tile 1 TQPED**			2.8V ; 27 mA				
Pin(SG)	**Pout(PS)**	**Pin(corr)**	**Pout(corr)**	**Gain**	**I1(2.8V)**	**PDC(mw)**	**Pout(mw)**	**Drn Eff**	**PAE**
-10.0	4.96	-10.10	5.06	15.16	26.7	74.7	3.21	4.3	4.2
-8.0	6.92	-8.10	7.02	15.12	26.9	75.2	5.04	6.7	6.5
-6.0	8.84	-6.10	8.94	15.04	27.2	76.2	7.83	10.3	10.0
-4.0	10.66	-4.10	10.76	14.86	27.8	77.7	11.91	15.3	14.8
-2.0	12.45	-2.10	12.55	14.65	28.8	80.7	17.99	22.3	21.5
0.0	14.11	-0.10	14.21	14.31	30.7	86.0	26.36	30.6	29.5
1.0	14.83	0.90	14.93	14.03	32.0	89.6	31.12	34.7	33.4
2.0	15.48	1.90	15.58	13.68	33.4	93.4	36.14	38.7	37.0
3.0	15.95	2.90	16.05	13.15	34.6	96.7	40.27	41.6	39.6
4.0	16.35	3.90	16.45	**12.55**	35.6	**99.6**	**44.16**	44.3	**41.9**
5.0	16.64	4.90	16.74	**11.84**	36.2	**101.4**	**47.21**	46.5	**43.5**
6.0	16.86	5.90	16.96	11.06	36.5	102.2	49.66	48.6	44.8

Table 2. Measured power performance of 1st pass ARL08M450.

450 MHz	PKG#8A	**PA450MHz Emode ARL #8 Tile 1 TQPED**			2.8V ; 26 mA				
Pin(SG)	**Pout(PS)**	**Pin(corr)**	**Pout(corr)**	**Gain**	**I1(2.8V)**	**PDC(mw)**	**Pout(mw)**	**Drn Eff**	**PAE**
-10.0	4.24	-10.10	4.34	14.44	26.4	73.8	2.72	3.7	3.5
-8.0	6.18	-8.10	6.28	14.38	26.5	74.2	4.25	5.7	5.5
-6.0	8.10	-6.10	8.20	14.30	26.8	74.9	6.61	8.8	8.5
-4.0	9.91	-4.10	10.01	14.11	27.2	76.2	10.02	13.2	12.6
-2.0	11.64	-2.10	11.74	13.84	27.9	78.1	14.93	19.1	18.3
0.0	13.14	-0.10	13.24	13.34	28.9	80.9	21.09	26.1	24.9
1.0	13.77	0.90	13.87	12.97	29.4	82.4	24.38	29.6	28.1
2.0	14.35	1.90	14.45	12.55	30.0	84.0	27.86	33.2	31.3
3.0	14.82	2.90	14.92	12.02	30.5	85.3	31.05	36.4	34.1
4.0	15.2	3.90	15.3	**11.40**	30.8	**86.2**	**33.88**	39.3	**36.5**
5.0	15.46	4.90	15.56	**10.66**	30.8	**86.3**	**35.97**	41.7	**38.1**
6.0	15.63	5.90	15.73	9.83	30.6	85.7	37.41	43.7	39.1

Using the Cripps method (from Steve Cripps), the first step in the amplifier design was to pick a PHEMT device size for 50 mW and 100 mW of RF output power biased with a 2.8-V supply. The 1st pass amplifier used a 0.5-mm PHEMT (6x80 µm), which should provide 50 mW for a 2.8-V supply (figure 3). Doubling the amplifier PHEMT size (10x96 µm) should increase the output power to the desired 100-mW goal for a 2.8-V supply (figure 4).

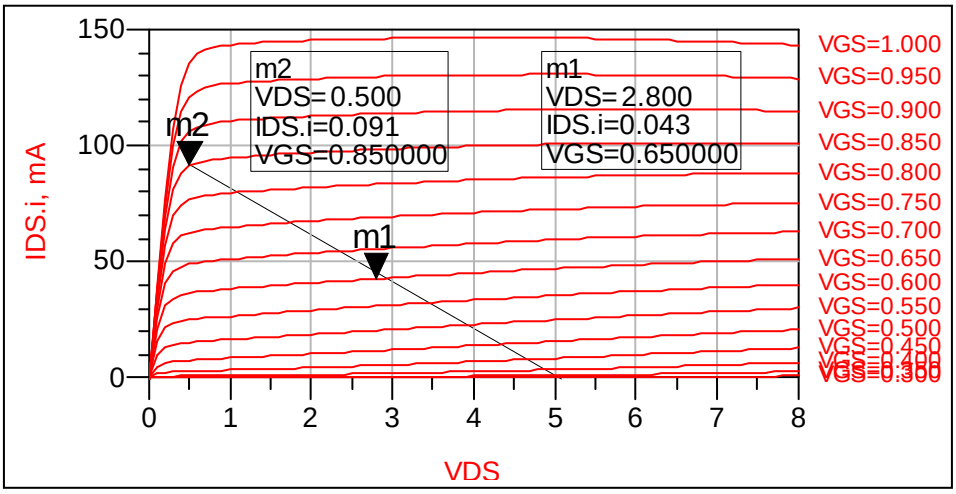

Figure 3. Cripps load line for a 50-mW PA (6x80 µm PHEMT with a 2.8-V supply).

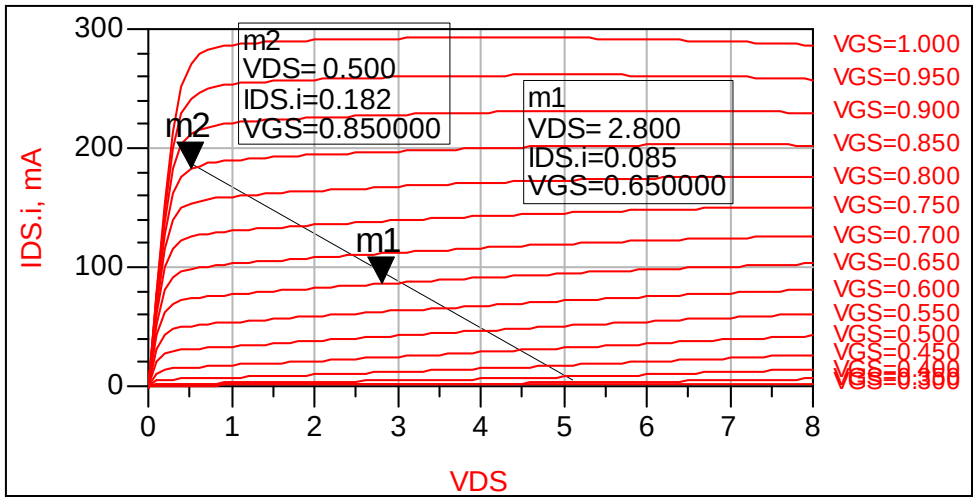

Figure 4. Cripps load line for a 100-mW PA (10x96 µm PHEMT with a 2.8-V supply).

AWR's MWO was used to simulate the initial narrowband amplifier designs, with some additional simulations using Agilent's ADS for comparison. Sonnet software was used to verify the layout using an electromagnetic (EM) simulation of the individual circuit layouts combined with transistor models of the PHEMTs. Figure 5 shows the schematic of the 100-mW (2.8-V), 425-MHz power amplifier from MWO. Simulations show that the amplifier provides 100 mW of output power with greater than 50% PAE at 400 and 450 MHz with 0-dBm input (1-mW) at 2.8 V and a small signal IDS of 78 mA. The amplifier has a lot of gain at low frequencies, in fact, the original stabilizing resistors were changed slightly after the design review to provide some additional margin, dropping the gain slightly (figure 6). Power performance was simulated and was shown to meet the goals of 100 mW and 50% PAE, as shown in figure 7. Figure 8 shows the dynamic load line of the amplifier PHEMT. Table 3 summarizes the 100-mW, 425-MHz power amplifier performance. A layout of the amplifier as a probable test cell included in the tile is shown in figure 9. There was an additional small pad and resistor added after the design review that is not shown in this plot that allows monitoring of the gate bias and also a means to bypass the current mirror circuit during testing.

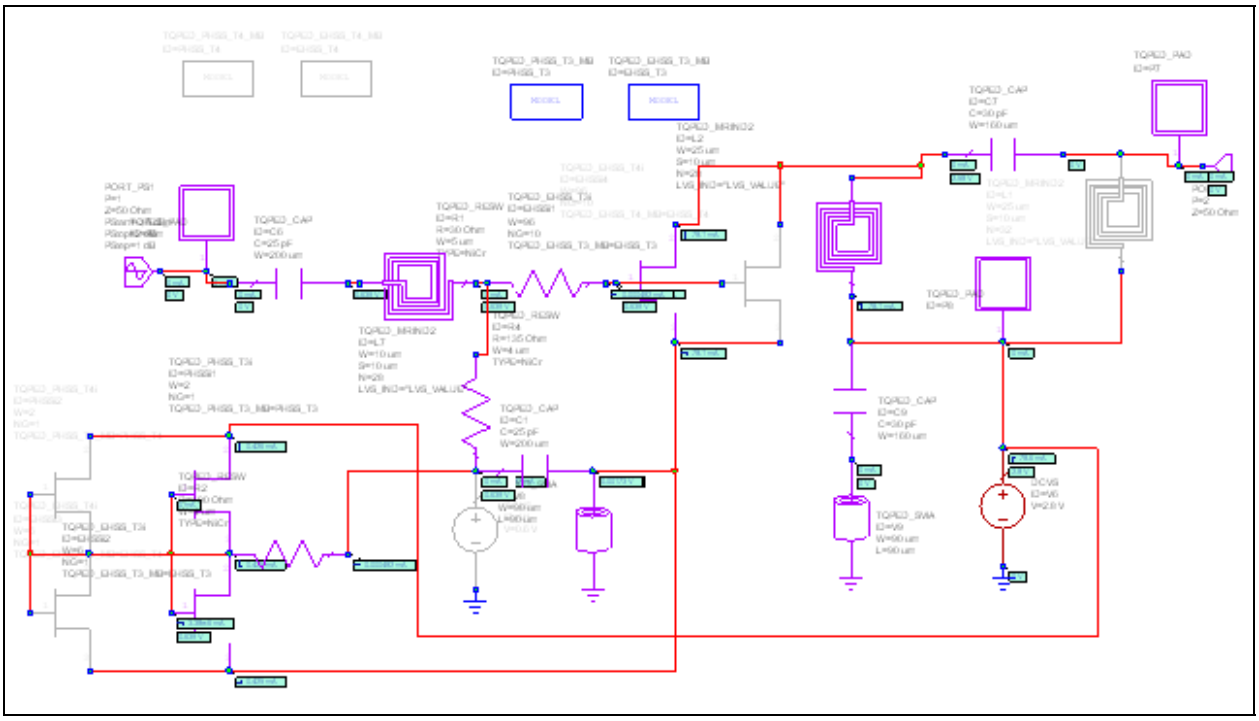

Figure 5. Schematic of 100-mW, 2.8-V power amplifier (MWO).

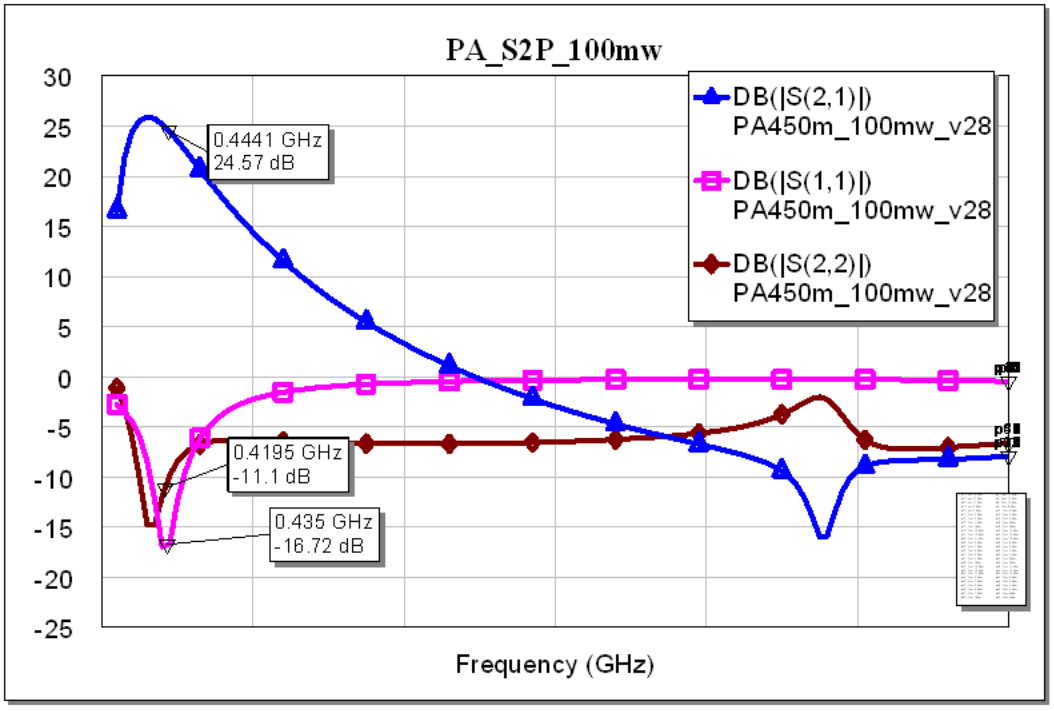

Figure 6. S-parameter simulation of 100-mW, 2.8-V power amplifier (MWO).

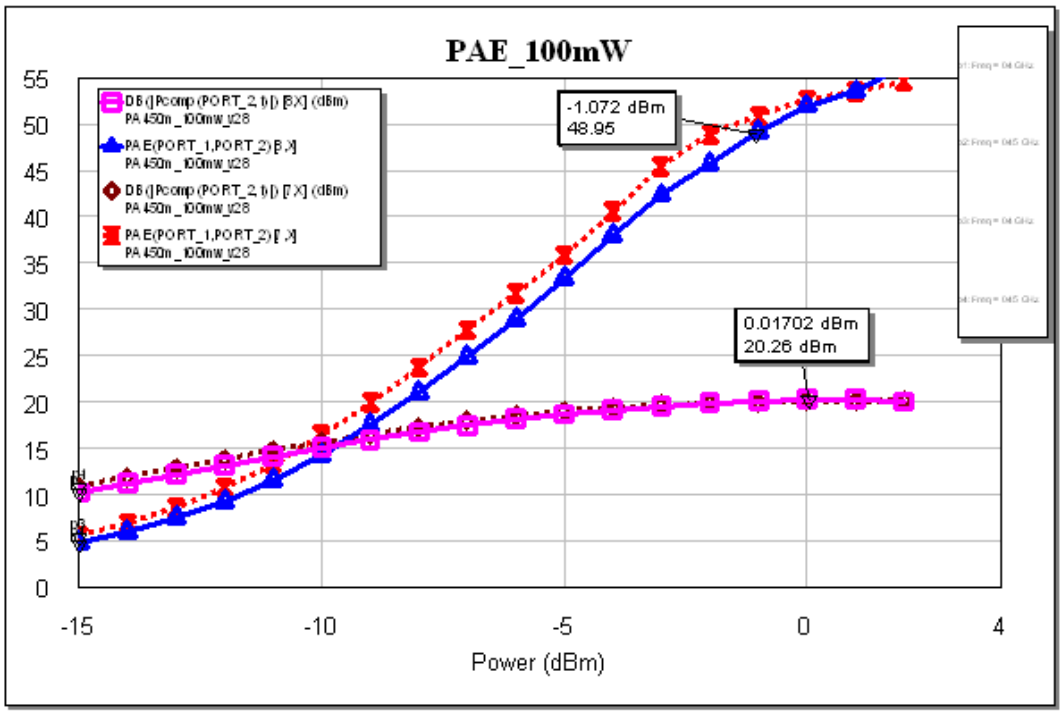

Figure 7. Power performance simulation of 100-mW, 2.8-V power amplifier (400 and 450 MHz).

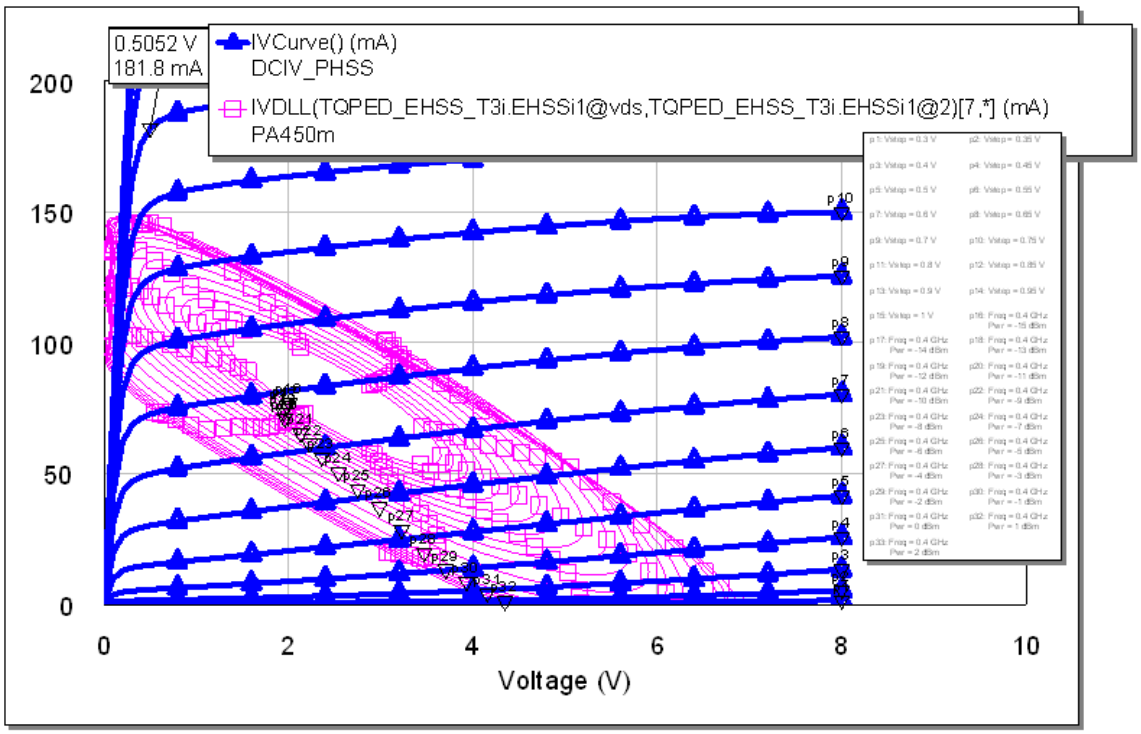

Figure 8. Dynamic load line simulation of 100-mW, 2.8-V power amplifier (MWO).

Table 3. Simulated performance of 425-MHz, 100-mW power amplifier.

Power (dBm)	Pout 0.45 GHz	PAE 0.45 GHz	Pout 0.40 GHz	PAE 0.4 GHz
–10	14.3682	12.1759	15.0634	14.2445
–9	15.2921	15.0109	15.9557	17.4261
–8	16.1622	18.2815	16.7791	21.0045
–7	16.9601	21.9035	17.508	24.8799
–6	17.6728	25.7596	18.1425	28.8796
–5	18.2811	29.879	18.6907	32.9027
–4	18.789	34.3215	19.1363	37.3061
–3	19.2284	38.8689	19.4856	42.1762
–2	19.6223	42.9513	19.7429	46.7506
–1	19.9386	46.9051	19.8992	49.6577
0	**20.1529**	**50.1867**	**19.9999**	**51.5825**
1	20.2823	52.5203	20.0418	53.2254
2	20.3495	53.8208	20.0678	54.1865

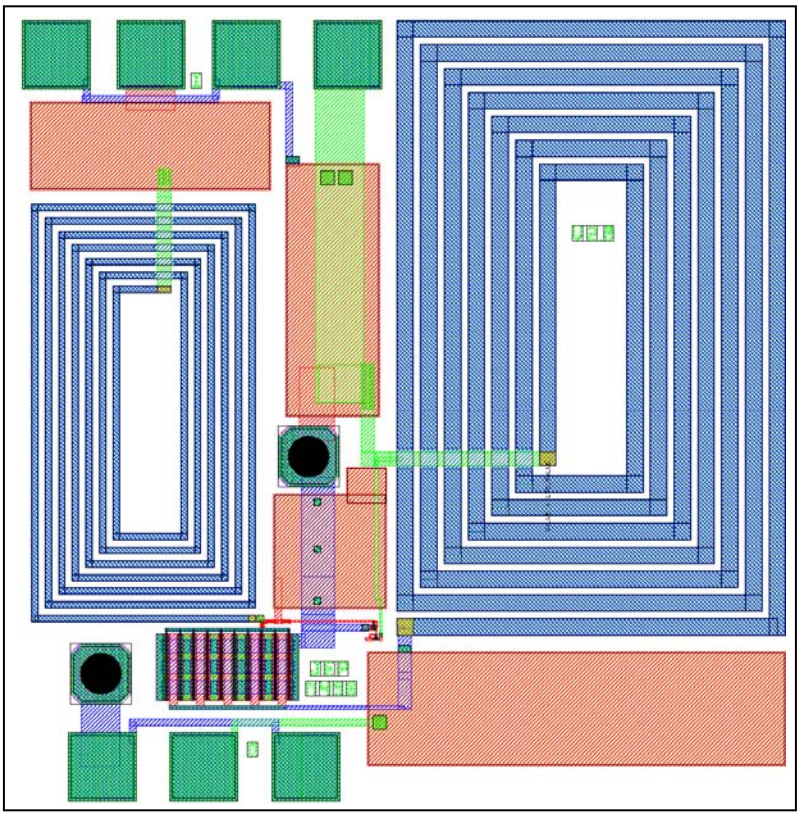

Figure 9. Layout of 100-mW, 2.8-V power amplifier (1.15x1.15 mm).

Another narrowband power amplifier was also designed with a goal of 50-mW output power and 50% PAE using a 2.8-V supply for half the DC power consumption of the 100 mW PA. Figure 10 shows the schematic of the narrowband 50-mW (2.8-V), 425-MHz power amplifier from MWO. Simulations show that the amplifier provides more than 50 mW of output power with greater than 50% PAE at 400 and 450 MHz with 0-dBm input (1-mW) at 2.8 V and a small signal IDS of 39 mA. An S-parameter simulation of the design shows good gain and input return

loss (figure 11). Power performance was simulated and was shown to meet the goals of 50 mW and 50% PAE as shown in figure 12. Table 4 summarizes the 50-mW, 425-MHz power amplifier performance. A layout of the amplifier as a probe-able test cell included in the tile is shown in figure 13. There was an additional small pad and resistor added after the design review that is not shown in this plot that allows monitoring of the gate bias and also a means to bypass the current mirror circuit during testing.

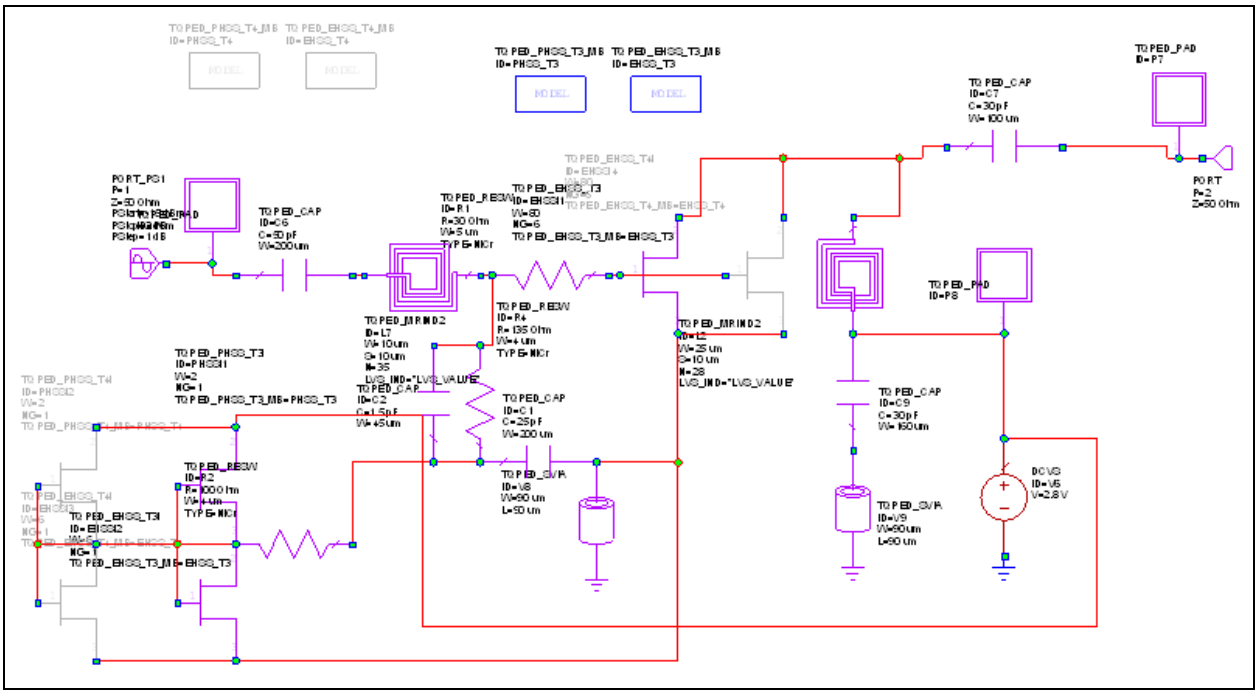

Figure 10. Schematic of 50-mW narrowband, 2.8-V power amplifier (MWO).

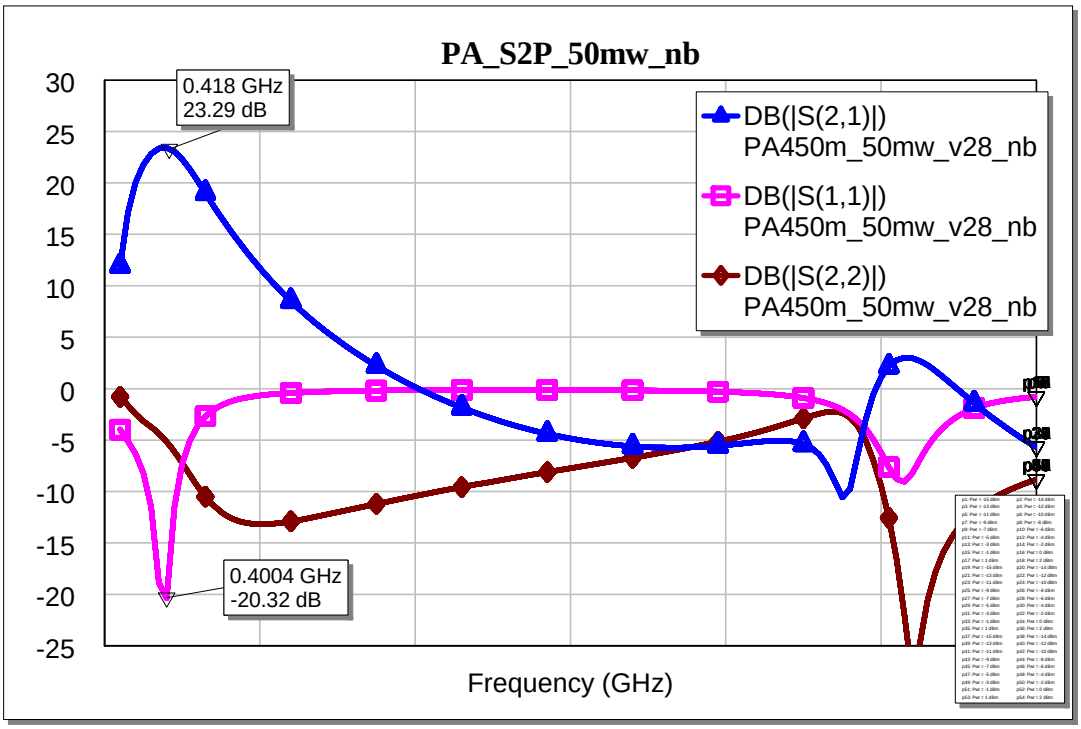

Figure 11. S-parameter simulation of 50-mW narrowband, 2.8-V power amplifier (MWO).

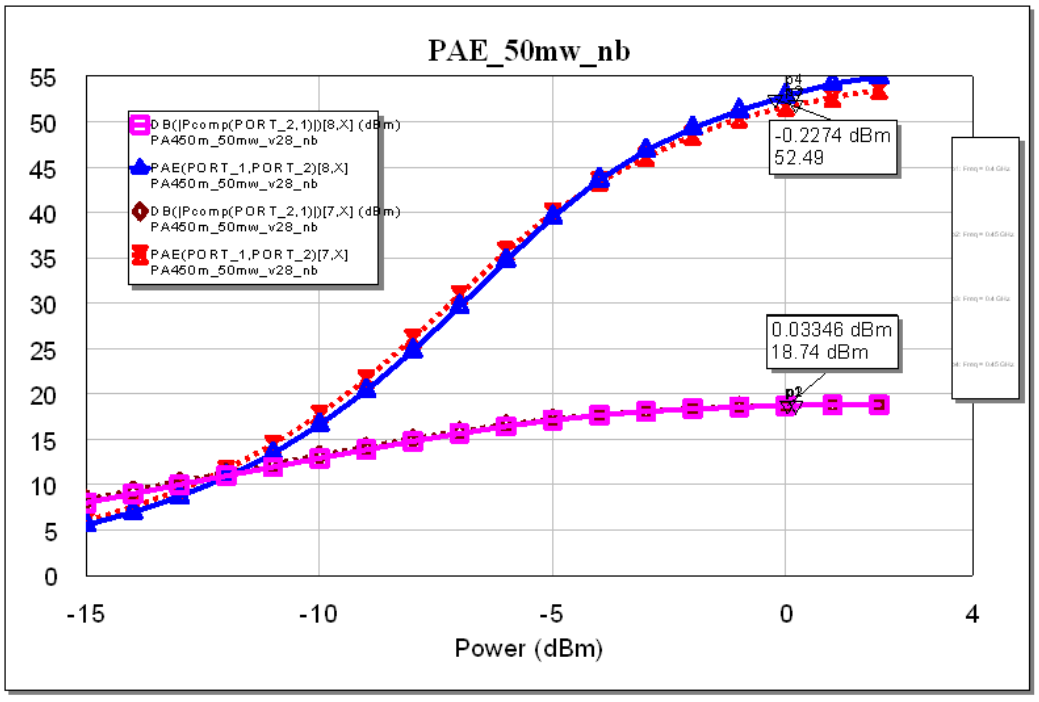

Figure 12. Power performance simulation of 50-mW narrowband, 2.8-V power amplifier (400 and 450 MHz).

Table 4. Simulated performance of the 425-MHz, 50-mW power amplifier.

Power (dBm)	Pout 0.45 GHz	PAE 0.45 GHz	Pout 0.40 GHz	PAE 0.4 GHz
–10	12.908	16.5759	13.2341	17.7262
–9	13.8551	20.3447	14.1645	21.6288
–8	14.7739	24.7309	15.0595	26.0825
–7	15.6435	29.6207	15.8954	30.9007
–6	16.4307	34.6991	16.6432	35.7074
–5	17.111	39.4916	17.2594	39.9942
–4	17.6743	43.607	17.7144	43.4018
–3	18.0763	46.8375	18.0745	46.1309
–2	18.3511	49.3081	18.3943	48.4815
–1	18.5574	51.2367	18.6227	50.3712
0	**18.7138**	**52.8591**	**18.7428**	**51.6878**
1	18.7881	54.2084	18.7925	52.6691
2	18.7931	54.93	18.7907	53.5416

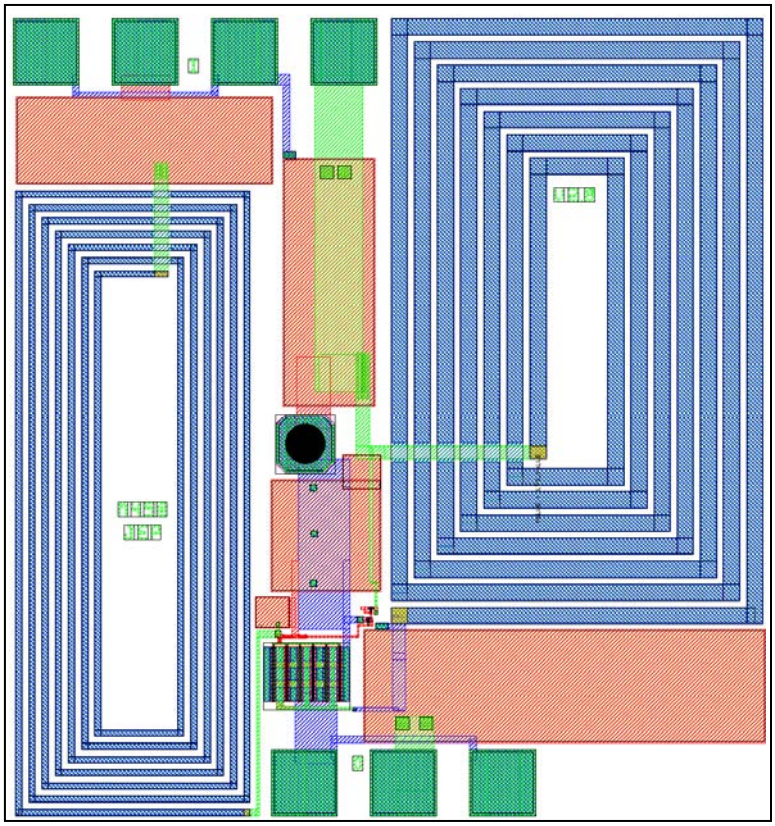

Figure 13. Layout of the 50-mW, 2.8-V narrowband power amplifier (1.15x1.2 mm).

The power amplifier from the 1st pass was reused to provide a broadband design as well as to provide a 50-mW design for operation with a 3.6-V battery. This design was already shown to have excellent gain and efficiency but some minor improvements were made to increase the efficiency. The shunt stabilizing resistor was DC blocked with a large capacitor to improve the efficiency a few percent by removing the 1-mA parasitic current flow. Also, the current mirror

was reduced from a 5- to a 2-µm device reducing that parasitic current from 1 to 0.4 mA, which should add a couple of percent to the efficiency. Figure 14 shows the schematic of the broadband 50-mW (2.8/3.6-V) power amplifier from MWO. Simulations show that the amplifier provides almost 50 mW of output power with about 47% PAE at 400 and 450 MHz with 0-dBm input (1-mW) at 2.8 V. An S-parameter simulation of the design shows good gain over a broad frequency range (figure 15). Power performance was simulated and was shown to be close to the goals of 50 mW and 50% PAE as shown in figure 16. Table 5 summarizes the broadband PA performance. A layout of the amplifier is shown in figure 17, but was not included as a separate test cell since it is only slightly modified from the successful 1st pass design. There was an additional small pad and resistor added after the design review in the full chip design that allows monitoring of the gate bias and also a means to bypass the current mirror circuit during testing.

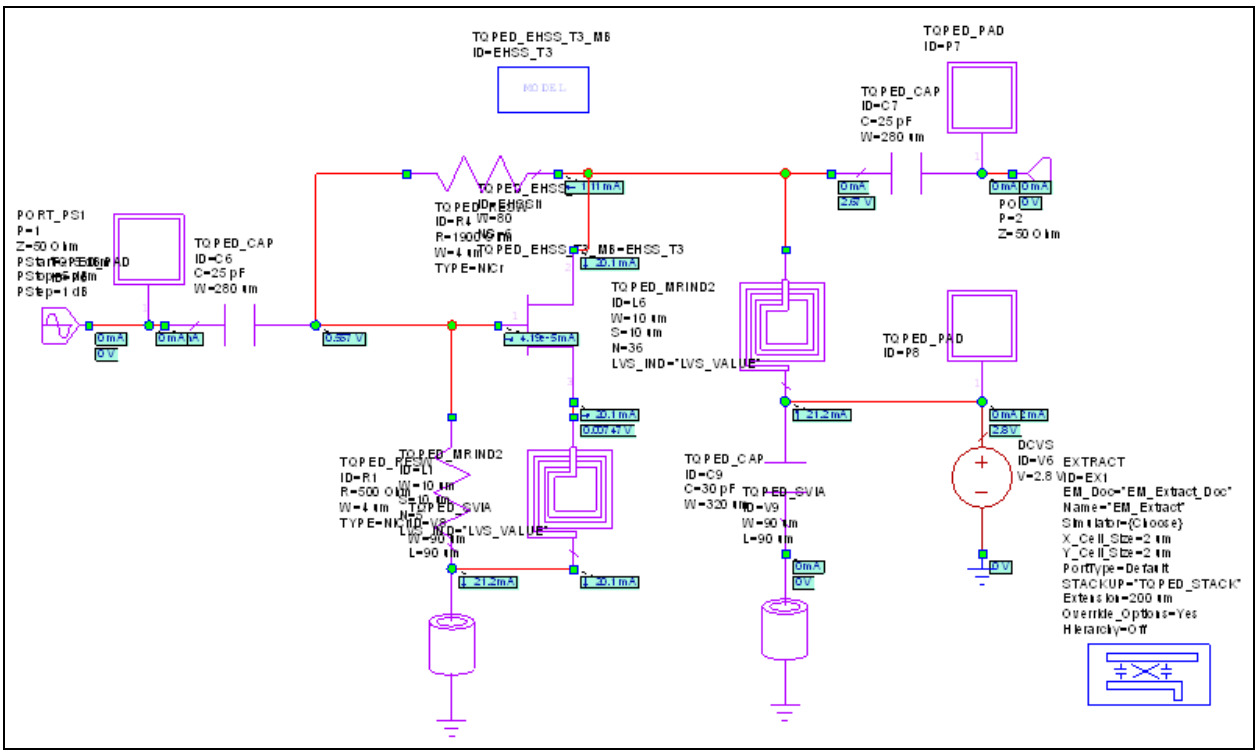

Figure 14. Schematic of the 50-mW broadband, 2.8-V power amplifier (MWO).

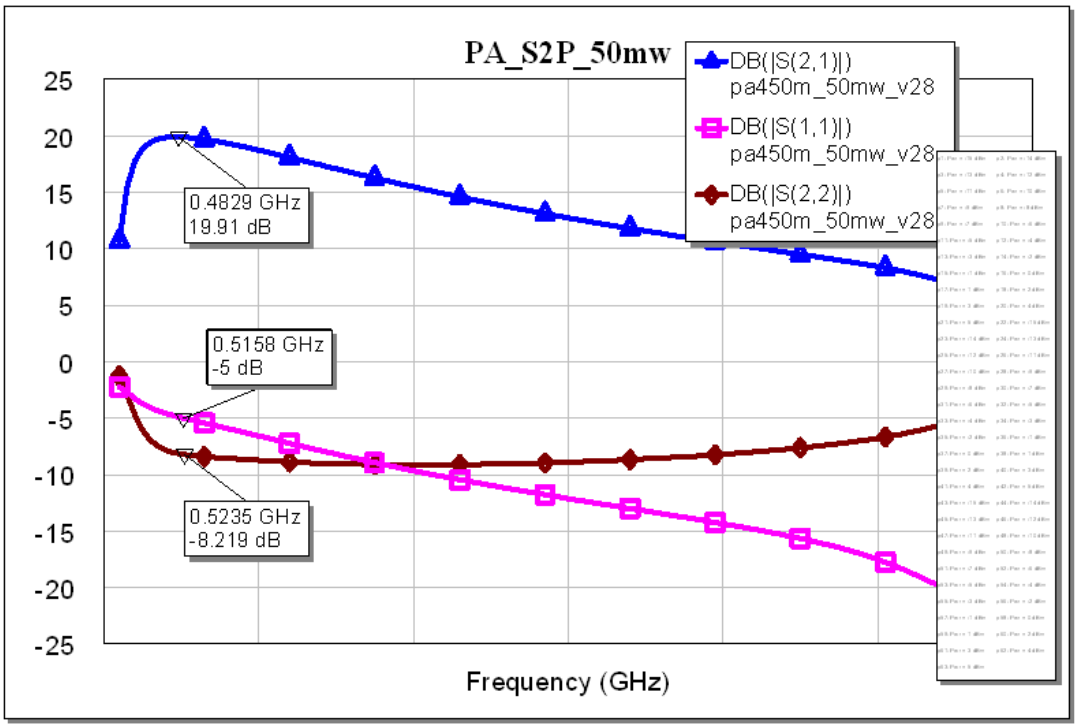

Figure 15. S-parameter simulation of the 50-mW broadband, 2.8-V power amplifier (MWO).

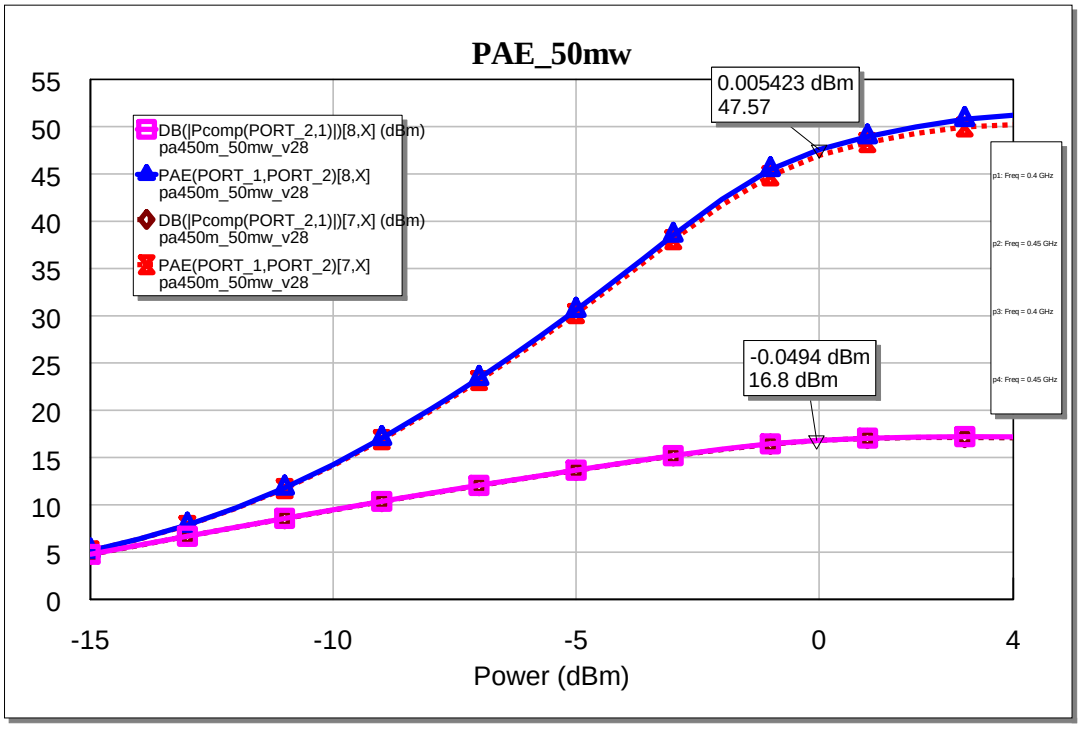

Figure 16. Power performance simulation of the 50-mW broadband, 2.8-V power amplifier (400 and 450 MHz).

Table 5. Simulated performance of broadband PA.

Power (dBm)	Pout 0.45 GHz	PAE 0.45 GHz	Pout 0.40 GHz	PAE 0.4 GHz
–10	9.47886	14.2564	9.45505	14.1451
–9	10.366	17.0402	10.3397	16.8885
–8	11.2249	20.1022	11.1965	19.9017
–7	12.0566	23.3937	12.027	23.1408
–6	12.8676	26.8906	12.8376	26.5813
–5	13.6657	30.6024	13.6359	30.2382
–4	14.4509	34.5239	14.422	34.1011
–3	15.2038	38.5338	15.1754	38.0493
–2	15.8872	42.3231	15.8435	41.7069
–1	16.4552	45.4821	16.4097	44.8043
0	**16.8231**	**47.5654**	**16.8025**	**46.9706**
1	17.05	48.9521	17.0187	48.321
2	17.1761	49.9858	17.116	49.2891

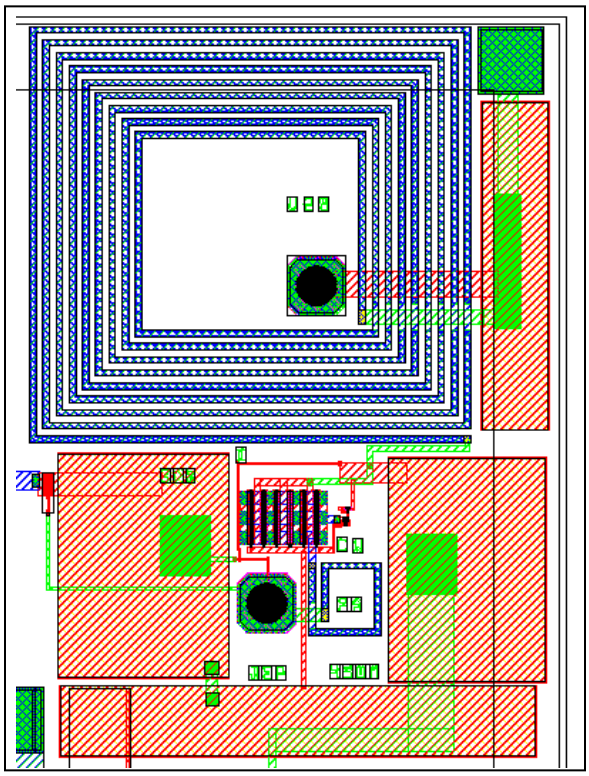

Figure 17. Layout of the 50-mW broadband, 2.8-V power amplifier (0.8x1.1 mm).

A low DC current consumption narrowband low noise amplifier was designed similar to the 1st pass design with a goal of a 2-dB noise figure and current consumption around 3 mA using the smaller 0.4-mA (2-µm PHEMT) current mirror for a very robust DC bias for supplies of 2 to 5 V. Figure 18 shows the schematic of the narrowband 425-MHz low noise amplifier from MWO. Simulations show that the amplifier provides about 11 dB of gain with an IDS of 3.2 mA

at 2.8 V (figure 19). Noise figure simulations show that the design should meet the goal of 2 dB as shown in figure 20. Table 6 summarizes the low noise amplifier performance. A layout of the low noise amplifier as a probe-able test cell is shown in figure 21. For the low noise amplifier, there was no need to add an extra test pad and resistor to bypass the current mirror circuit since the concern was only for large signal operation of the power amplifier. Table 6 summarizes the low noise amplifier performance.

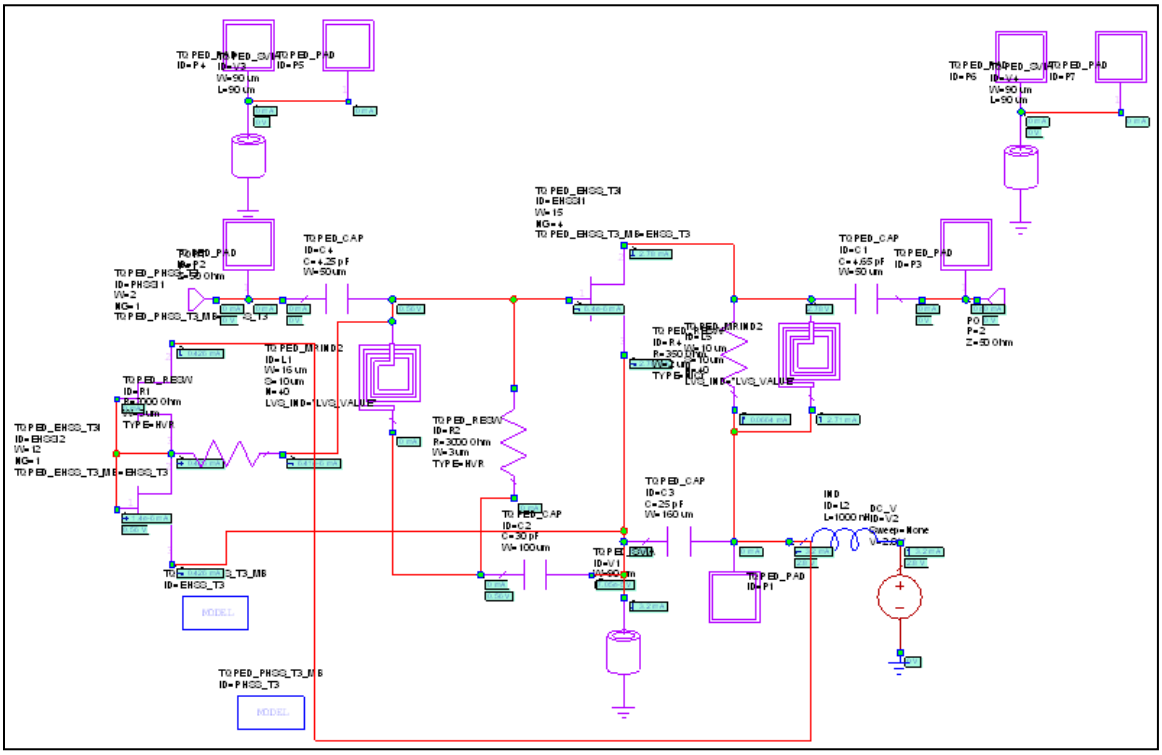

Figure 18. Schematic of the 425-MHz low noise amplifier (MWO).

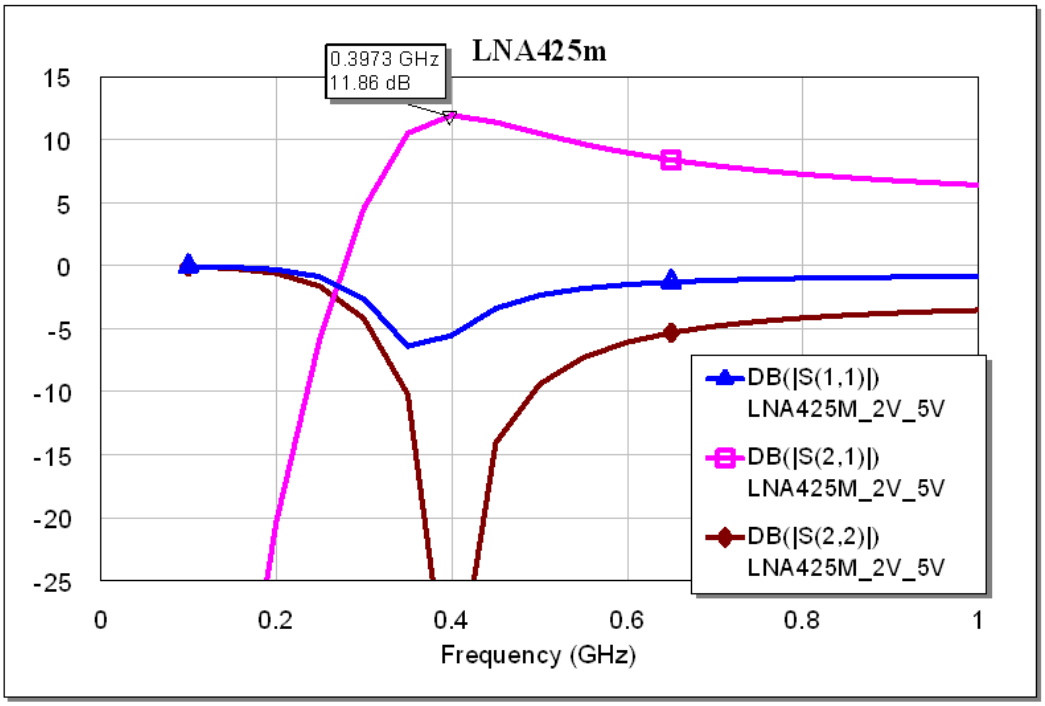

Figure 19. S-parameter simulation of the 425-MHz low noise amplifier (MWO).

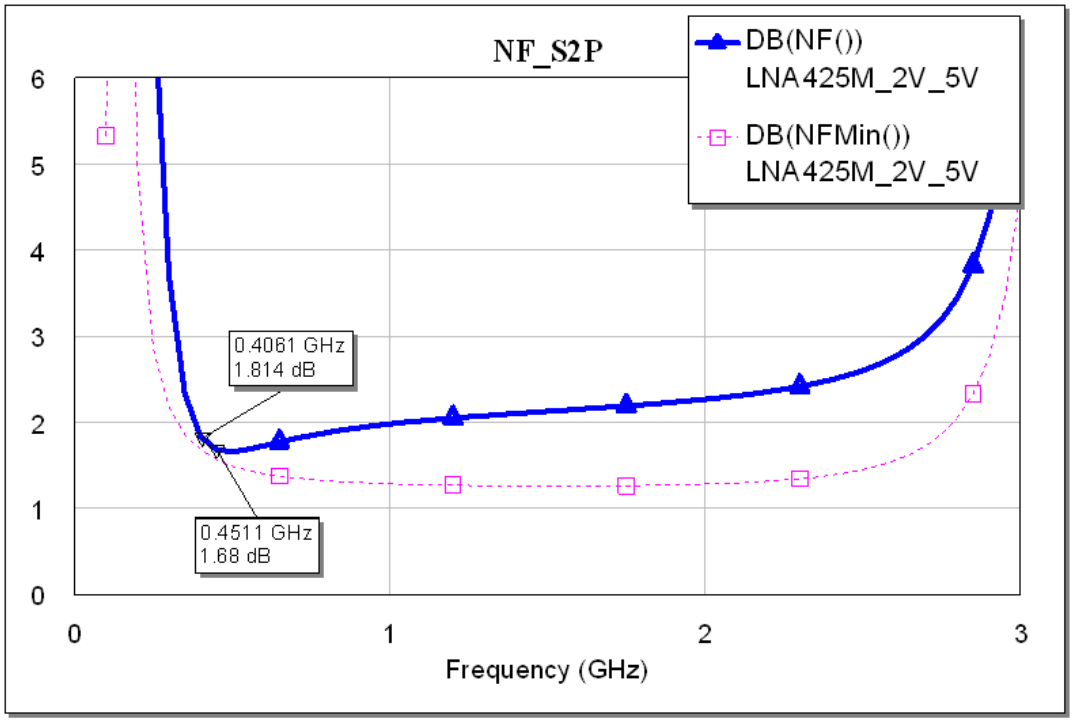

Figure 20. Noise figure simulation of the 425-MHz low noise amplifier (MWO).

Table 6. Simulated performance of the 425-MHz low noise amplifier.

Frequency (GHz)	DB(NF())	DB(|S(2,1)|)
0.3	3.69481	4.5861
0.35	2.32686	10.5096
0.4	1.83241	11.9386
0.45	1.68046	11.3902
0.5	1.65716	10.4841
0.55	1.68343	9.64657
0.6	1.72521	8.95129
0.65	1.76856	8.38857
0.7	1.80916	7.93259
0.75	1.84617	7.55922
0.8	1.87904	7.2503
0.85	1.90819	6.99148
0.9	1.9341	6.77191
0.95	1.95741	6.58272
1	1.97845	6.41824

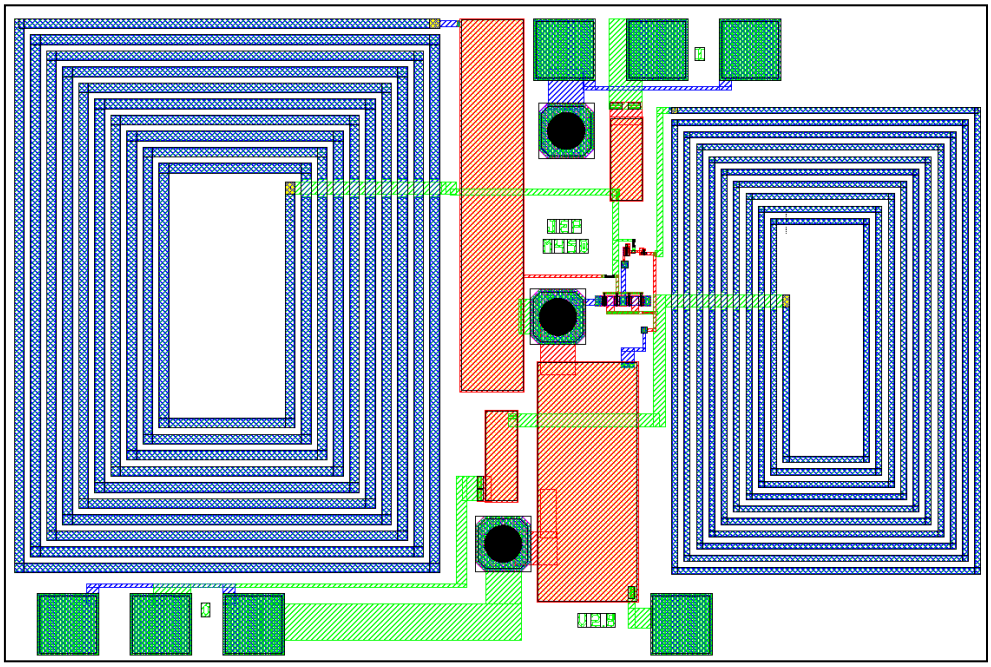

Figure 21. Layout of the 425-MHz low noise amplifier (1.6x1.0 mm).

A broadband positive voltage control TR switch from the 1st pass was redesigned to reduce the higher than desired insertion loss with a goal of 0.5 dB. First, the PHEMT switches were doubled in size to reduce the inherent series resistance of the switches. Some test switch devices from the Johns Hopkins University MMIC Design Fall 2009 student designs showed that a switch using devices similar in size to those in ARL's 1st pass had an insertion loss of 0.5 dB and using switches twice as big reduced the insertion loss to less than 0.2 dB as measured. Another source

of loss in the ARL 1st pass designs was too much use of the lossy thin metal0 layer, so care was taken in the 2nd pass design to transition from metal0 to the thicker metal1 or metal2 layers for connections. In order to make the dmode PHEMTs take positive voltage control signals, large capacitors are needed. The size of the capacitors is a tradeoff between size and insertion loss. Overall the insertion loss is expected to be close to 0.5 dB, about half due to the capacitor size tradeoff and half due to the lossy PHEMT switches. Figure 22 shows the schematic of the broadband TR switch from MWO. Simulations show that the insertion loss is around 0.5 dB (figure 23). Large signal power simulations show that the design should be able to handle 100 mW of power without compressing (figure 24). A layout of the broadband TR switch as a probe-able test cell is shown in figure 25. The two way switch either goes to a 50-ohm resistor to ground to measure isolation, or to a through path to measure insertion loss. A reference voltage must be supplied (typically 2.5 V) to use a positive control voltage for the dmode PHEMTs in the TR switch.

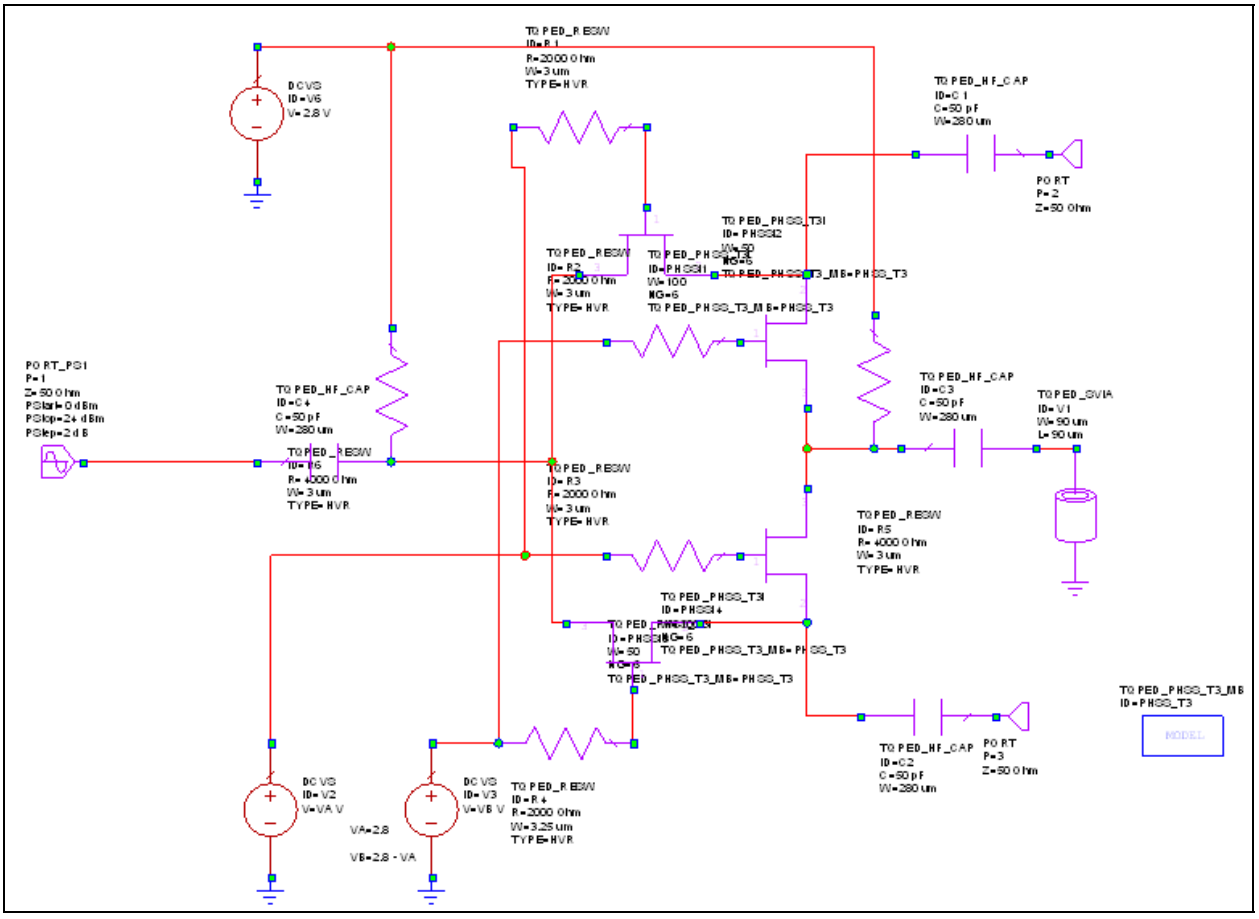

Figure 22. Schematic of the broadband TR switch (MWO).

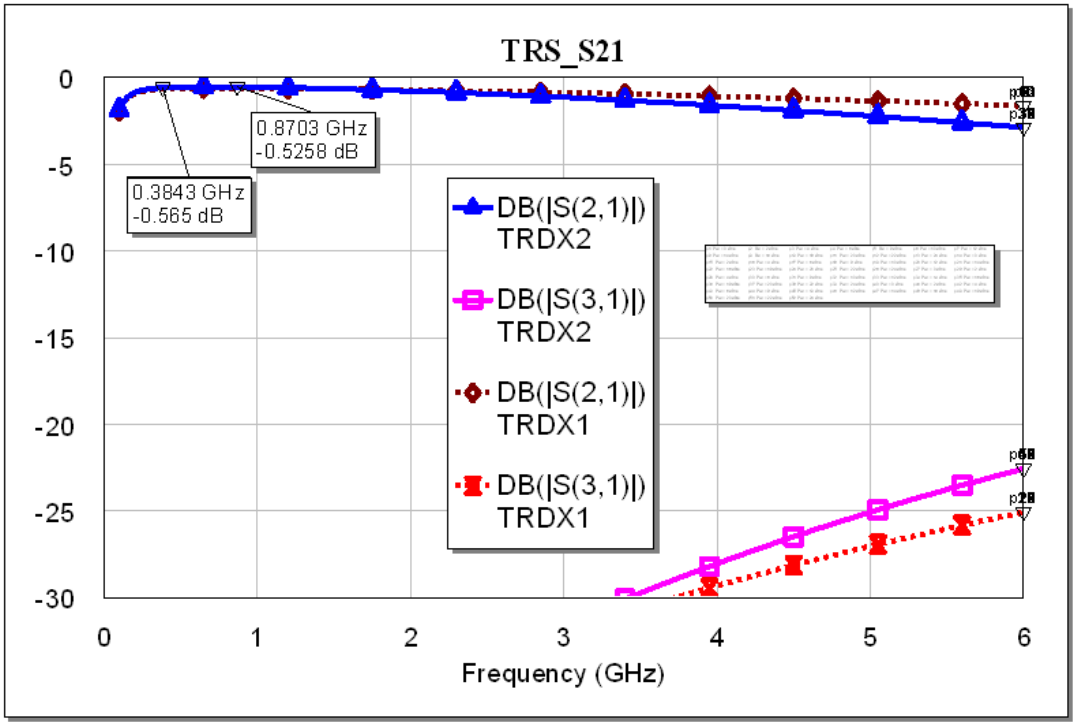

Figure 23. S-parameter simulation of the broadband TR switch (MWO).

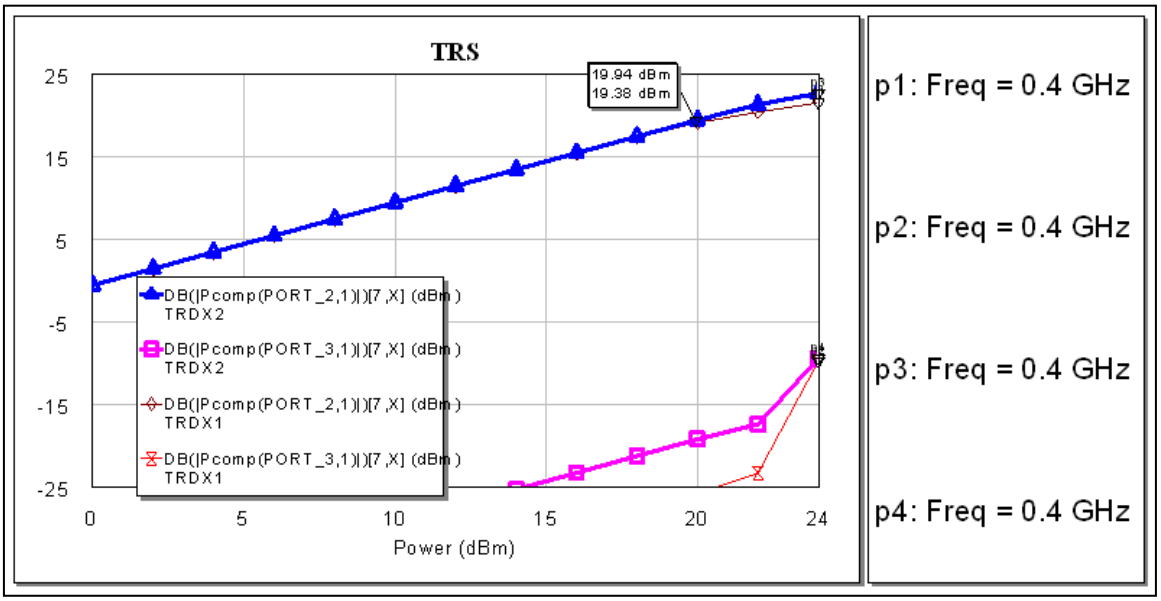

Figure 24. Power performance simulation of the broadband TR switch (MWO).

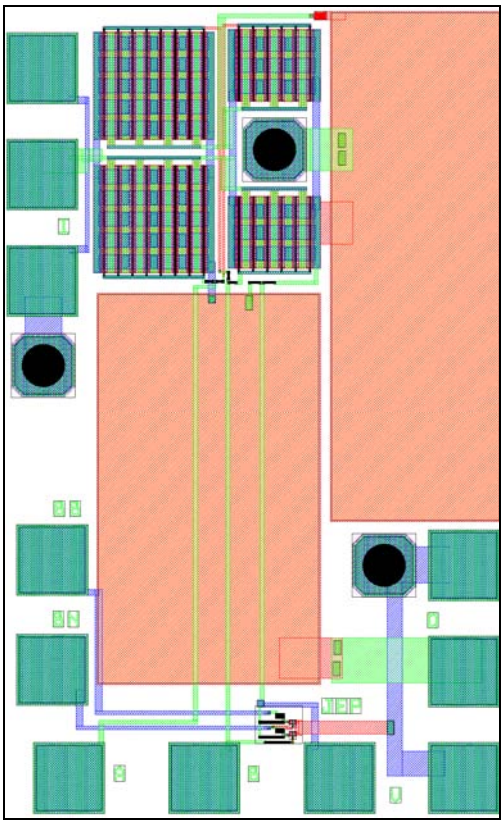

Figure 25. Layout of the broadband TR switch
(probe-able test cell—0.7x1.1 mm).

The BPSK modulator from the 1st pass worked very well and was only slightly retuned for a center frequency of 425 MHz versus the previous 450 MHz. A second broader band design was created using 5 elements in the high pass and low pass networks that are switched to create the two modulation states. To minimize the number of inductors, the low pass network was modified from three series inductors with two shunt capacitors to two series inductors with three shunt capacitors to save space. Simulations of the dual band or broadband BPSK modulator are shown in figures 26 and 27. The layout of the dual band BPSK modulator included in a full IC design is shown in figure 28.

A broadband low noise amplifier was needed for the dual band design, so the high current high gain broadband low noise amplifier design from the 1st pass was modified for use with similar performance but less current consumption than the original. The current mirror was modified to reduce the current consumption from 16 mA to about 8 to 10 mA with a slight drop in gain to about 15 dB at 425 and 900 MHz. Since this design is so similar to the previous design only its simulation in the top level full IC designs will be shown.

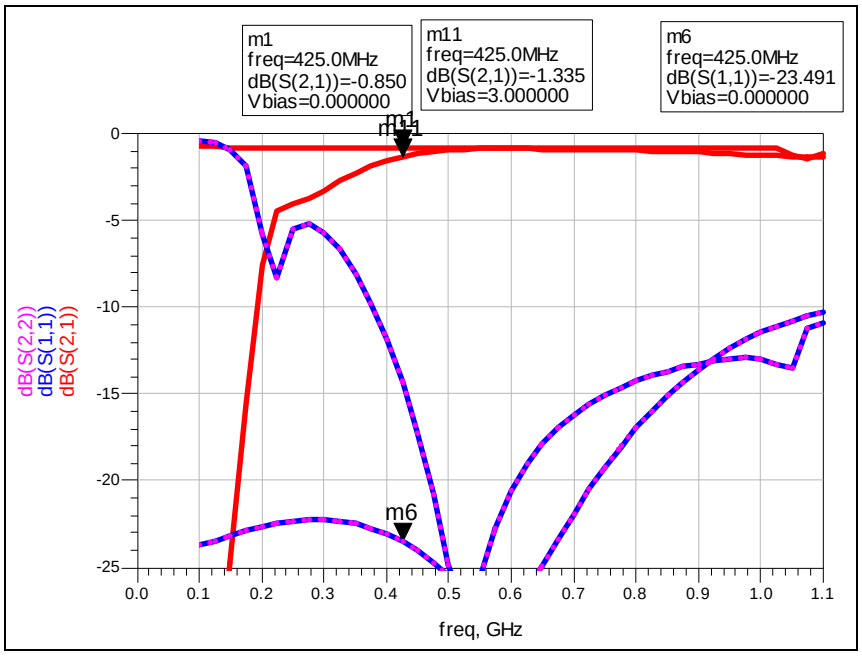

Figure 26. Insertion loss simulation of the dual band BPSK modulator (ADS).

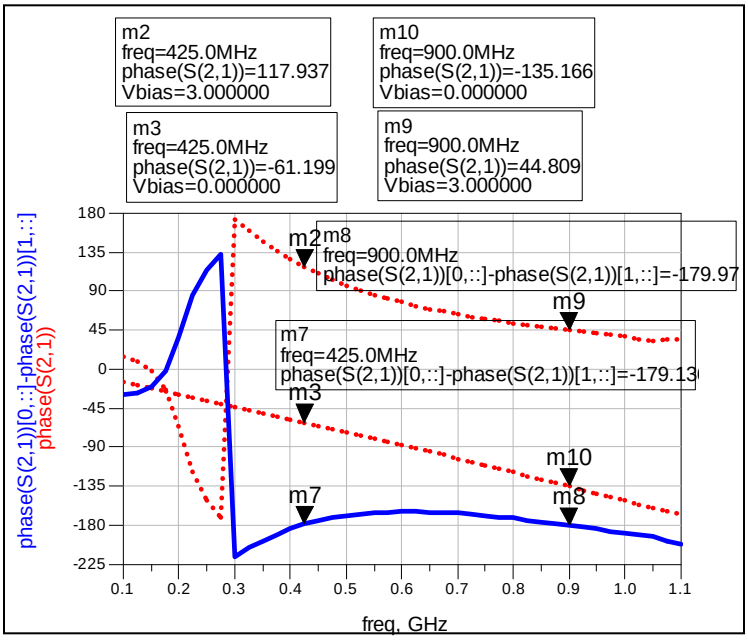

Figure 27. Phase difference simulation of the dual band BPSK modulator (ADS).

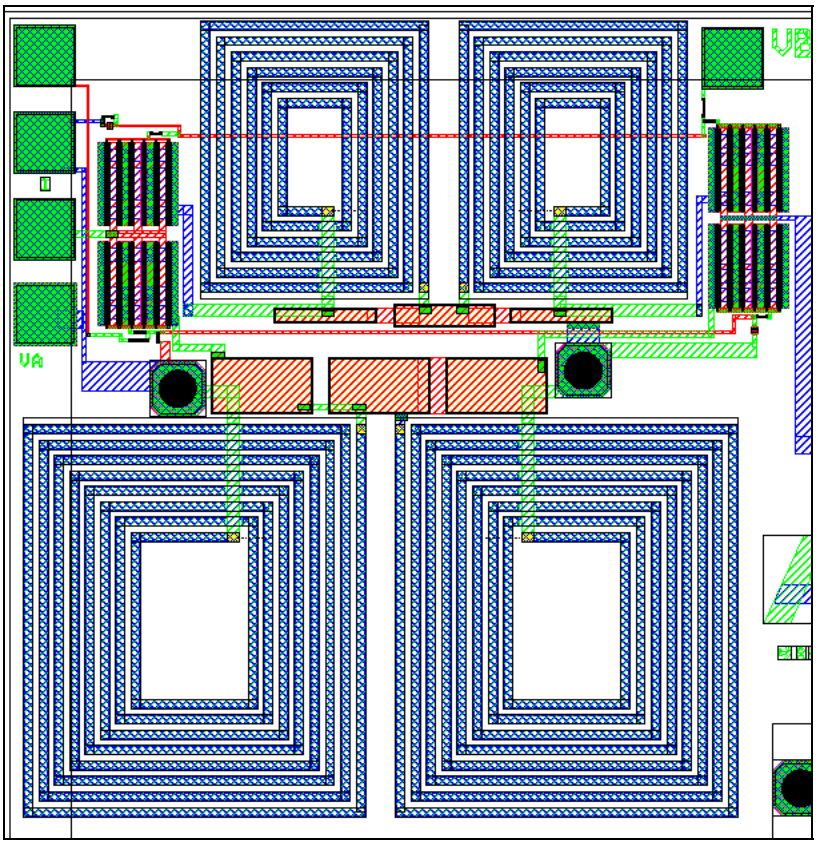

Figure 28. Layout of the dual band BPSK modulator (1.3x1.3 mm).

4. Active GaAs IC Designs

The focus of the 2nd pass was predominantly the 400 to 450 MHz frequency band, but there was also a desire to have a broadband or dual band application since the commercial RFICs are typically capable below 1 GHz with the proper external matching circuits, which then tend to narrowband the system design. As with the 1st pass tile, the designs were part of a multi-die fabrication so several active design variations were included to meet various design goals. Since the band of interest was lower in frequency and since inductors and capacitors grow in size as the frequency is lowered, the larger 4x4 mm QFN package was targeted for packaging the die. A 95x95 mil (2.41x2.41 mm) size was chosen. This could allow up to eight designs of this size to be included in a single quarter tile prototype fabrication. The previous 1st pass designs tried to maximize the number of design variations over many frequency bands and targeted either 3x3 or 4x4 mm QFN packages, such that only the BPSK modulator and power amplifier could be squeezed into the smaller die size at the lower frequency. The larger die size allowed for increasing the size of the lumped elements to retune designs to a slightly lower frequency

(425 MHz versus 450 MHz) and allowed for the inclusion of the modulator, power amplifier, TR switch, and low noise amplifier in a single die. There are four active design variations targeting 50 mW at 2.8 V, 100 mW at 2.8 V, at least 50 mW for either 2.8 V or 3.6 V, and a dual band design at 425 or 900 MHz using the broadband power amplifier design with a newly designed broadband BPSK modulator design. The fifth active design is a test circuit with the narrowband 50-mW power amplifier, the narrowband 100-mW power amplifier, the narrowband 3-mA low noise amplifier, and the broadband TR switch design for individual probe testing. Later, passive GaAs IC designs to improve the system level performance by integrating the external RFIC matching circuits into a single IC are discussed. Following is a brief description of each active design in the 2nd pass ARL tile following a similar naming convention to the 1st pass designs. The numbers start with 21 and go to 29 with some additional letters to designate frequency or other variations.

The following are descriptions of the active designs:

- ARL21M425—This 425-MHz design contains a BPSK modulator, a 100-mW power amplifier for 2.8 V, a narrowband low DC power consumption low noise amplifier, and a TR switch using positive voltage control inputs with negative threshold depletion PHEMTs. It is a 95x95 mil die.
- ARL22M425—This 425-MHz design contains a BPSK modulator, a 50-mW power amplifier for 2.8 V, a narrowband low DC power consumption low noise amplifier, and a TR switch using positive voltage control inputs with negative threshold depletion PHEMTs. It is a 95x95 mil die.
- ARL23M425—This 425-MHz design contains a BPSK modulator, a 50/75-mW power amplifier for 2.8/3.6 V, a narrowband low DC power consumption low noise amplifier, and a TR switch using positive voltage control inputs with negative threshold depletion PHEMTs. This design is intended to operate over a broader range of battery voltages. It is a 95x95 mil die.
- ARL24DB—This dual band design contains a BPSK modulator for 425 or 900 MHz, the broadband 50/75-mW power amplifier for 2.8/3.6 V, a broadband moderate DC power consumption low noise amplifier, and a TR switch using positive voltage control inputs with negative threshold depletion PHEMTs. This design is intended to operate at either the 425 or 900 MHz frequency bands. It is a 95x95 mil die.
- ARL25—This is a test circuit of the individual subcircuits from the previous four design variations. It contains a 100-mW power amplifier for 2.8 V, a 50-mW power amplifier for 2.8 V, a narrowband low DC power consumption low noise amplifier, and a TR switch. It is a 95x95 mil die.

The full designs were initially simulated in MWO, but then were re-simulated with ADS. It was easy to reuse the ADS templates from the 1st pass IC designs. As expected, results of the full IC with power amplifier, TR switch, BPSK modulator, and low noise amplifier are comparable to the combined individual simulations of the subcircuits.

All layouts were designed to a 2.41x2.41 mm die size to fit in the cavity of a 4x4 mm QFN package. RF input to the transmit chain is placed in the upper left of each layout. The RF output of the receive chain or low noise amplifier, is placed in the lower left of each layout. A common RF connection to the antenna is placed in the lower right of each layout. One intent of this layout is to separate the RF front end into a selectable module for a higher level package assembly. While the designs have similar layouts, one could interchange the designs depending on battery supply voltage (typically, 2.8 or 3.6 V), output power desired (currently 50 or 100 mW), and possibly frequency of operation (425 MHz, or both 425 and 900 MHz). Another goal of this design effort was to integrate the many lumped element matching circuits required as board level components for an RFIC transceiver into a single small IC package. The matching circuit portion of the tile of IC designs are discussed in a following section.

The design designated as ARL21M425 contains a BPSK modulator in the upper left of the layout, a power amplifier optimized for 100 mW at 2.8 V in the upper right of the layout, a TR switch in the lower right of the layout, and a low current (3-mA) low noise amplifier in the lower left of the layout (figure 29). A preliminary wire bond diagram of the die in a 4x4 mm SEMPAC, 20-pin, 4x4 mm QFN package is shown in figure 30.

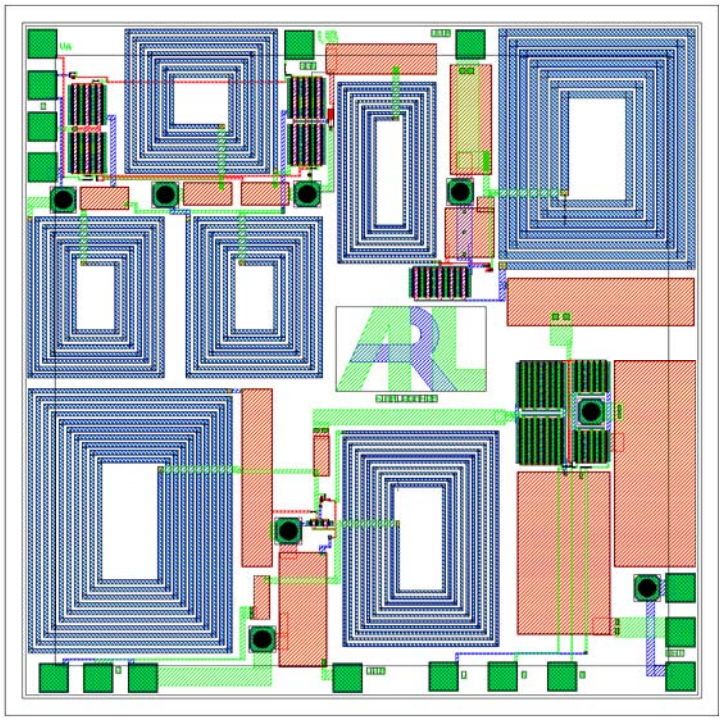

Figure 29. Layout of ARL21M425 (2.41x2.41 mm die).

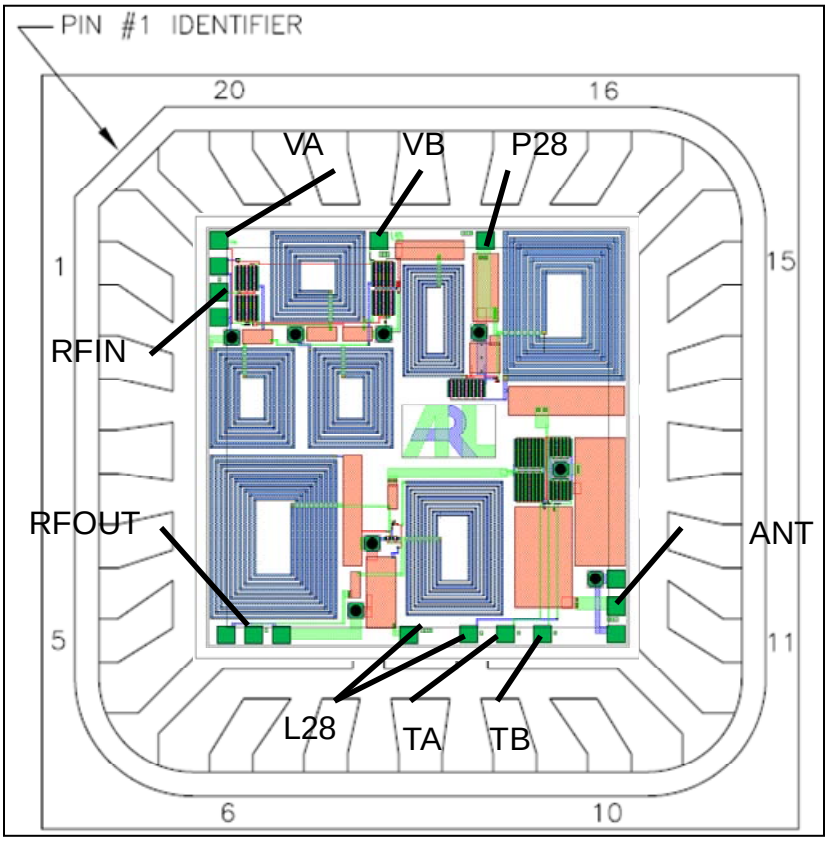

Figure 30. Wire-bond diagram of ARL21M425 in a 4x4 mm QFN package.

The design designated as ARL22M425 contains a BPSK modulator in the upper left of the layout, a power amplifier optimized for 50 mW at 2.8 V in the upper right of the layout, a TR switch in the lower right of the layout, and a low current (3-mA) low noise amplifier in the lower left of the layout (figure 31). A preliminary wire bond diagram of the die in a 4x4 mm SEMPAC, 20-pin, 4x4 mm QFN package is shown in figure 32. This design is identical to ARL21M425 except for the power amplifier which is targeted for half as much RF and DC power.

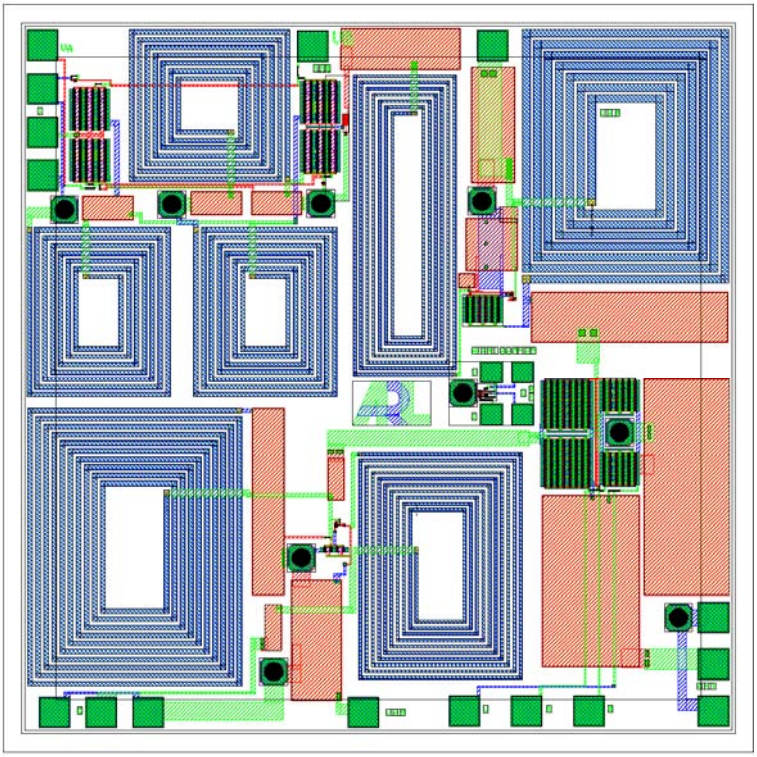

Figure 31. Layout of ARL22M425 (2.41x2.41 mm die).

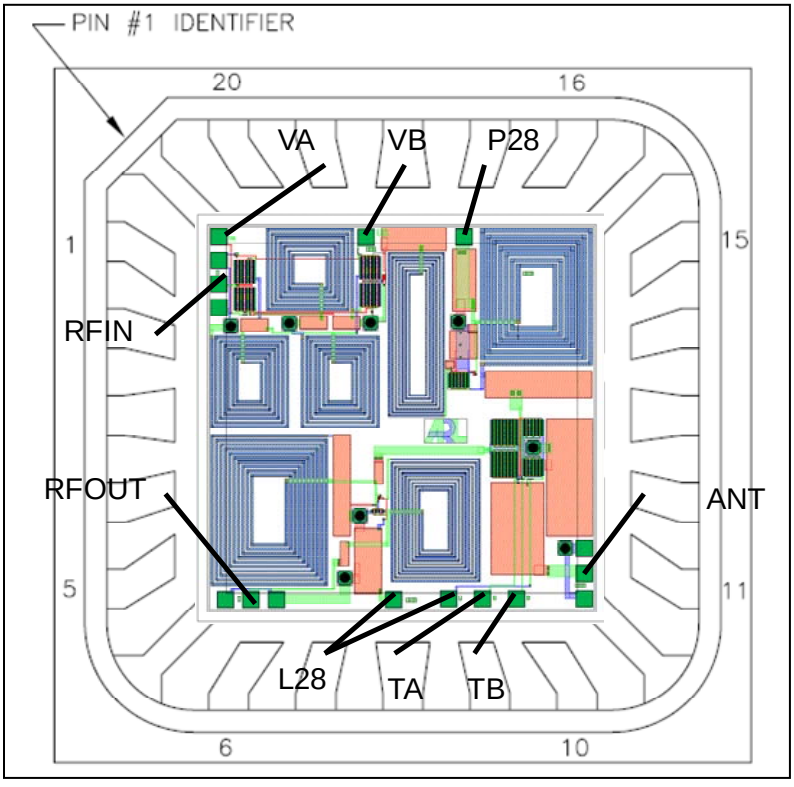

Figure 32. Wire-bond diagram of ARL22M425 in a 4x4 mm QFN package.

The design designated as ARL23M425 contains a BPSK modulator in the upper left of the layout, a broadband power amplifier optimized for 50 mW at 3.6 V in the upper right of the layout, a TR switch in the lower right of the layout, and a low current (3-mA) low noise amplifier in the lower left of the layout (figure 33). A preliminary wire bond diagram of the die in a 4x4 mm SEMPAC, 20-pin, 4x4 mm QFN package is shown in figure 34. This design is identical to ARL21M425 and ARL22M425 except for the broadband power amplifier whose design was used in the 1st pass designs. The power amplifier has good efficiency over a range of supply voltages but is expected to have less than the desired 50 mW of output power with a 2.8-V supply. If a 3.6-V supply is used, the output power should be greater than 50 mW with good efficiency.

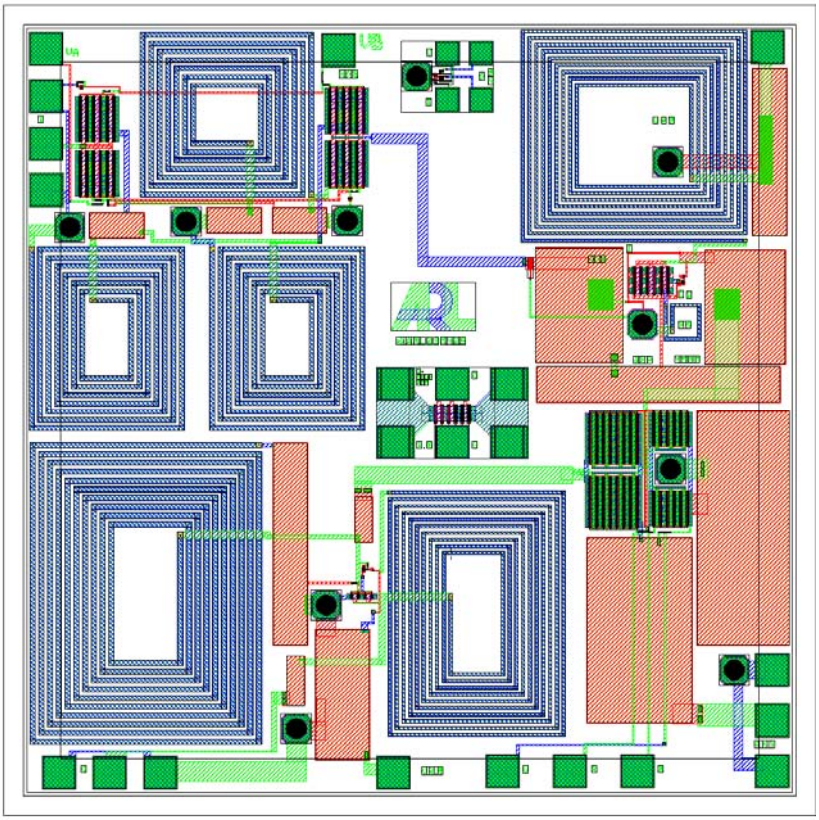

Figure 33. Layout of ARL23M425 (2.41x2.41 mm die).

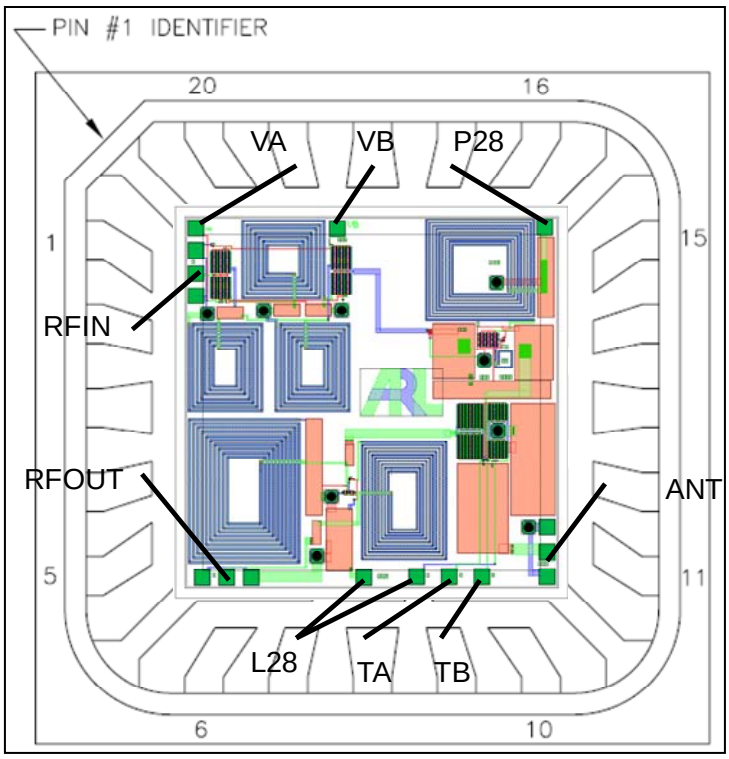

Figure 34. Wire-bond diagram of ARL23M425 in a 4x4 mm QFN package.

The design designated as ARL24DB contains a dual band 425/900-MHz BPSK modulator in the upper left of the layout, a broadband power amplifier optimized for 50 mW at 3.6 V in the upper right of the layout, a TR switch in the lower right of the layout, and a moderate current (9-mA) broadband low noise amplifier in the lower left of the layout (figure 35). A preliminary wire bond diagram of the die in a 4x4 mm SEMPAC, 20-pin, 4x4 mm QFN package is shown in figure 36. This design is similar to ARL23M425 except for the dual band BPSK modulator and the broadband higher current low noise amplifier, whose design was slightly modified from the broadband low noise amplifier in the 1st pass designs. As with ARL23M425, the power amplifier has good efficiency over a range of supply voltages but is expected to have less than the desired 50 mW of output power with a 2.8-V supply. If a 3.6-V supply is used, the output power should be greater than 50 mW with good efficiency. The broadband low noise amplifier uses more current than the narrowband 425-MHz design in the other three designs, but it is also expected to have 3 dB more of gain.

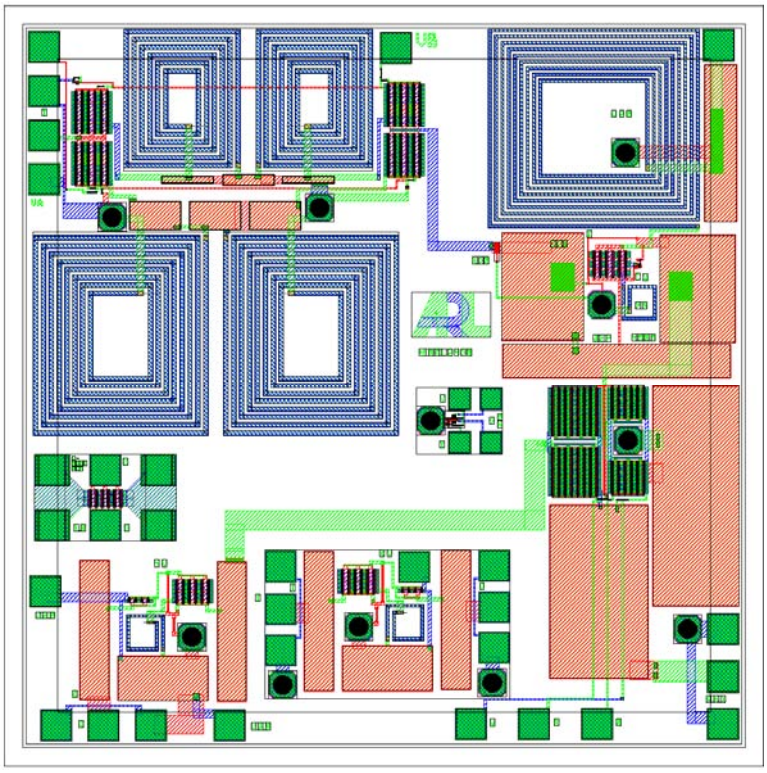

Figure 35. Layout of ARL24DB (2.41x2.41 mm die).

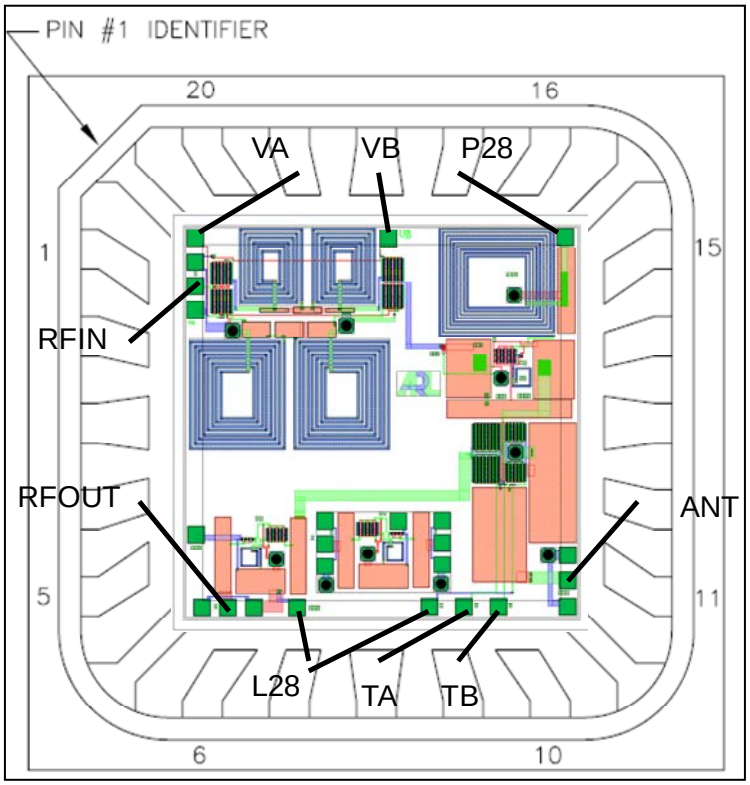

Figure 36. Wire-bond diagram of ARL24DB in a 4x4 mm QFN package.

The design designated as ARL25 has individual subcircuits for test. It contains a power amplifier optimized for 50 mW at 2.8 V (ARL22M425) in the upper left of the layout, a broadband power amplifier optimized for 100 mW at 2.8 V (ARL21M425) in the upper right of the layout, a TR switch in the lower right of the layout, and a low current (3-mA) low noise amplifier in the lower left of the layout (figure 37). Since this is a test circuit, a wire-bond diagram is not shown, but it could be packaged for individual subcircuit testing with wire bonds. Note that the layout of ARL24DB has a probe testable layout of the moderate current (9-mA) broadband low noise amplifier. The only subcircuits not directly testable as individual elements are the narrowband and dual band BPSK modulators.

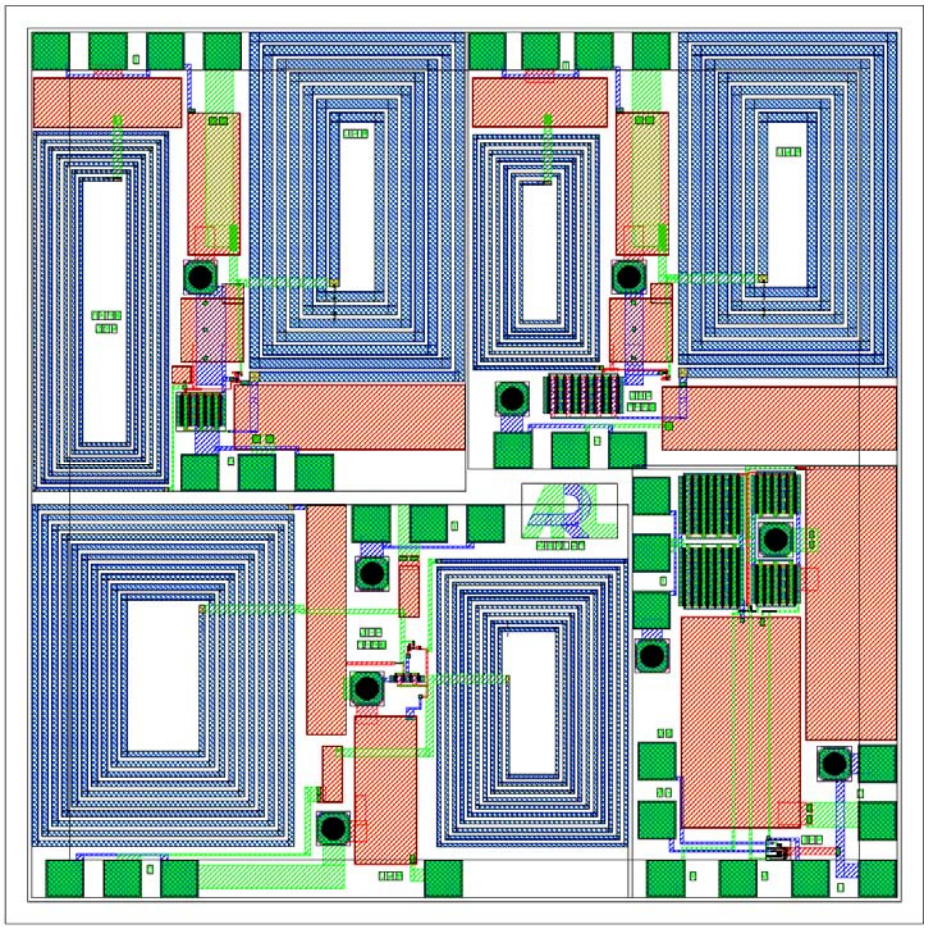

Figure 37. Layout of the ARL25 test cells (2.41x2.41 mm die).

The full IC designs were simulated to include the performance of the combined subcircuits, including the insertion loss affects of the TR switch. Figure 38 shows the full schematic of ARL21M425. A simulation of the transmit chain including the BPSK modulator, power amplifier, and TR switch is shown in figure 39. The receive chain simulation including the low noise amplifier and TR switch is shown in figure 40. Performance of the transmit and receive modes of ARL21M425 are shown in tables 7 and 8. As expected the output power, efficiency, and noise figure are slightly degraded by the insertion loss of the TR switch.

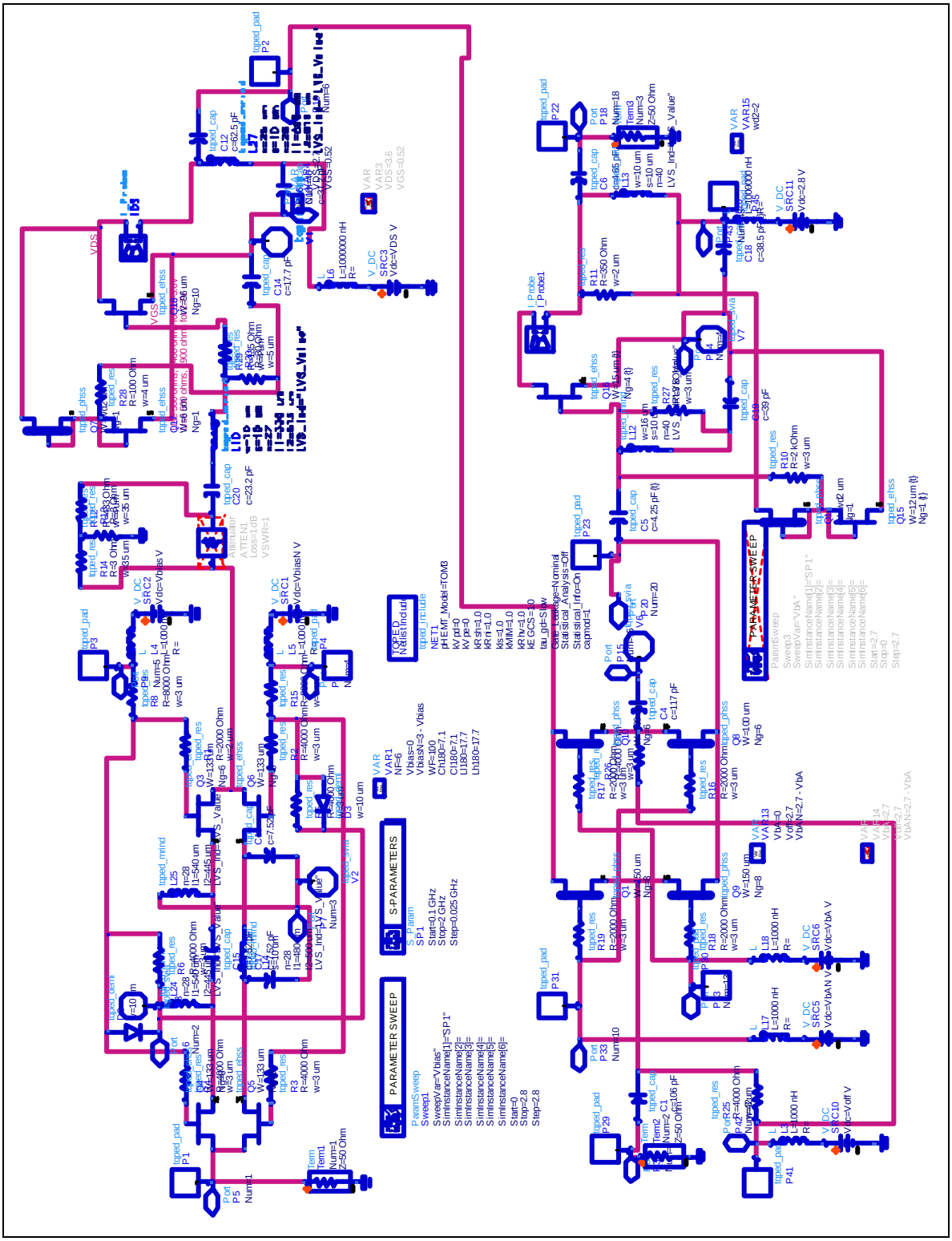

Figure 38. Schematic of ARL21M425, 100 mW and 2.8 V (ADS).

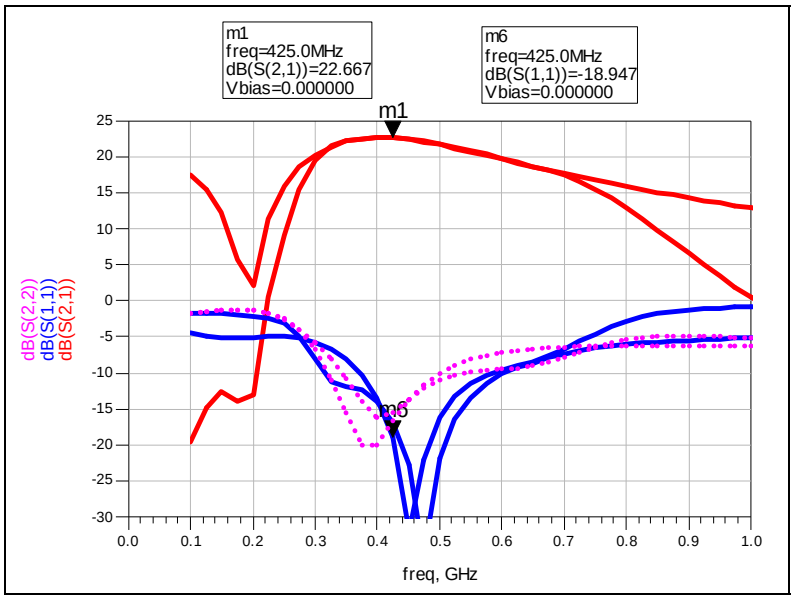

Figure 39. S-parameter simulation of ARL21M425 transmit (ADS).

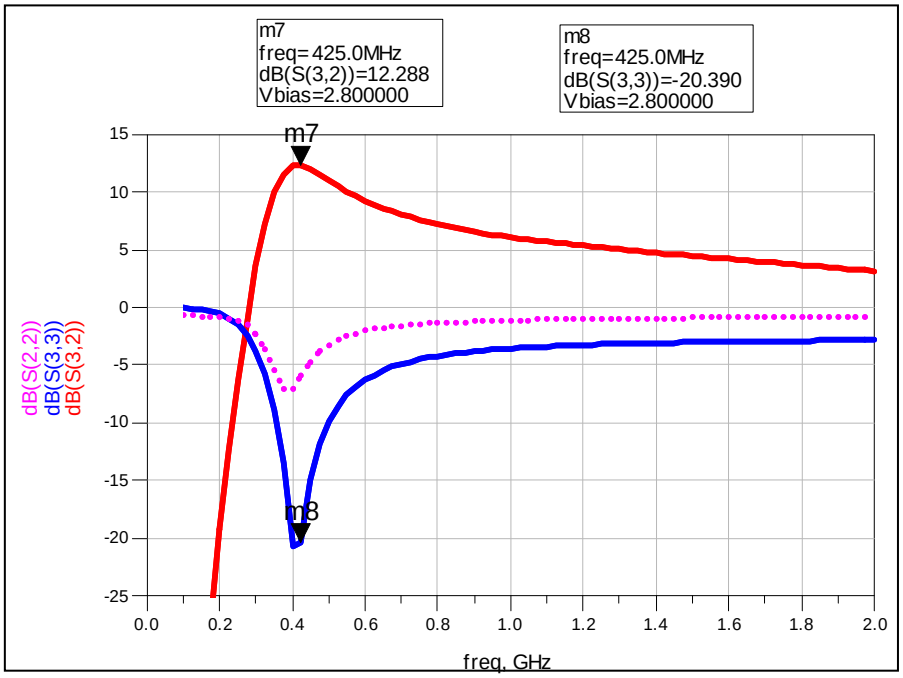

Figure 40. S-parameter simulation of ARL21M425 receive (ADS).

Table 7. Simulated performance of transmit chain for ARL21M425.

Power (dBm)	Pout 0.425 GHz	PAE 0.425 GHz	Gain 0.425 GHz
–16	6.66	2.36	22.66
–14	8.65	3.72	22.65
–12	10.64	5.86	22.64
–10	12.60	9.17	22.60
–8	14.51	14.12	22.51
–6	16.25	20.92	22.25
–4	17.66	28.89	21.66
–2	18.64	37.34	20.64
0	**19.39**	**44.22**	**19.39**
2	19.81	48.94	17.81

Table 8. Simulated performance of receive chain for ARL21M425.

Frequency (GHz)	DB(NF())	DB(|S(2,1)|)
0.3	5.21	3.54
0.35	3.34	9.96
0.4	**2.65**	**12.25**
0.45	**2.49**	**11.98**
0.5	2.54	11.04
0.55	2.65	10.09
0.6	2.77	9.28
0.65	2.89	8.61
0.7	3.01	8.06
0.75	3.12	7.60
0.8	3.23	7.21
0.85	3.32	6.88
0.9	3.40	6.59
0.95	3.47	6.33
1	3.53	6.10

Figure 41 shows the full schematic of ARL22M425. A simulation of the transmit chain including the BPSK modulator, power amplifier, and TR switch is shown in figure 42. The receive chain simulation including the low noise amplifier and TR switch is shown in figure 43. Performance of the transmit and receive modes of ARL22M425 are shown in tables 9 and 10. As expected the output power, efficiency, and noise figure are slightly degraded by the insertion loss of the TR switch.

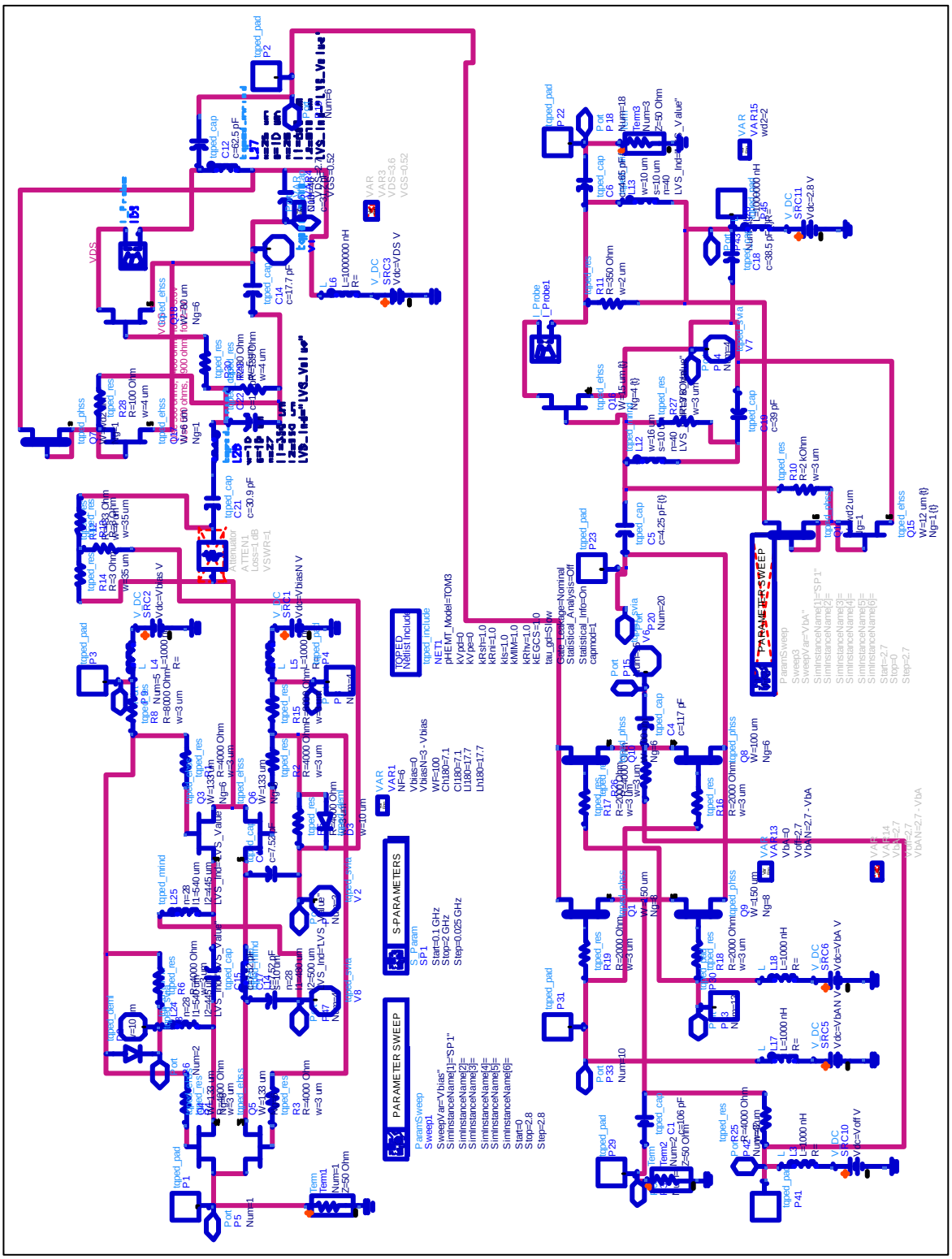

Figure 41. Schematic of ARL22M425 50 mW 2.8 V (ADS).

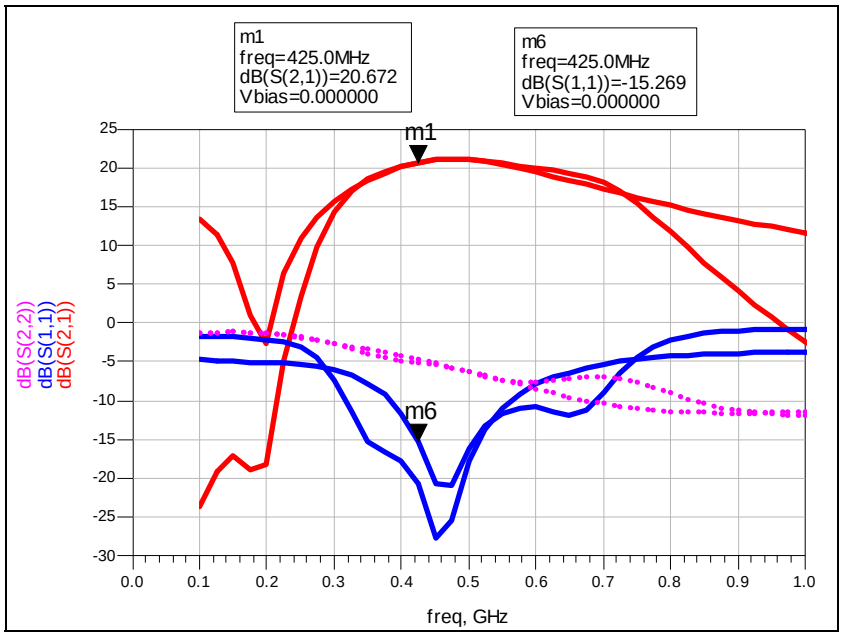

Figure 42. S-parameter simulation of ARL22M425 transmit (ADS).

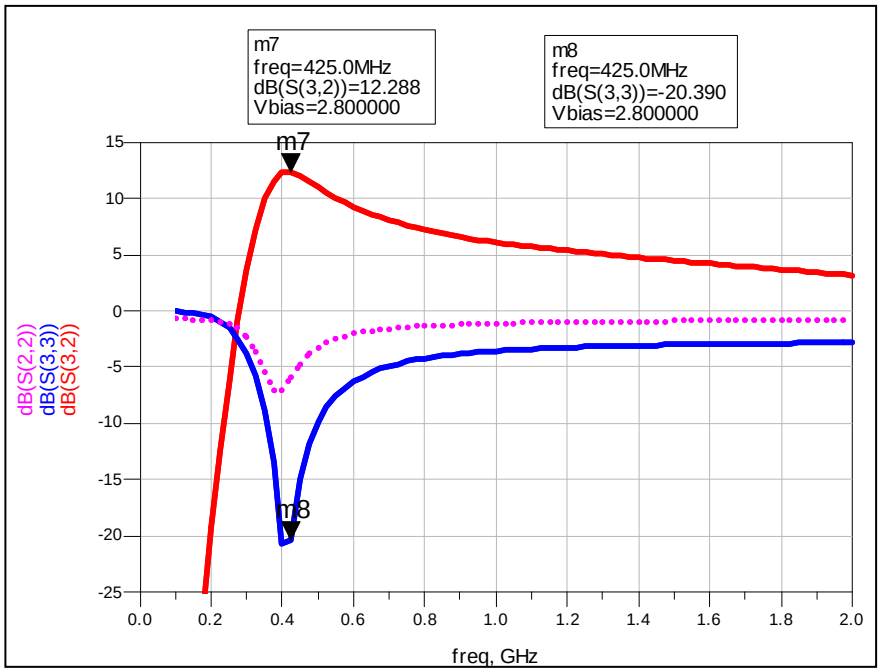

Figure 43. S-parameter simulation of ARL22M425 receive (ADS).

Table 9. Simulated performance of transmit chain for ARL22M425.

Power (dBm)	Pout 0.425 GHz	PAE 0.425 GHz	Gain 0.425 GHz
–16	4.64	2.81	20.64
–14	6.62	4.40	20.62
–12	8.58	6.85	20.58
–10	10.52	10.55	20.52
–8	12.41	15.92	20.41
–6	14.20	23.11	20.20
–4	15.75	31.16	19.75
–2	16.93	38.06	18.93
0	**17.76**	**43.19**	**17.76**
2	18.21	46.66	16.21

Table 10. Simulated performance of receive chain for ARL22M425.

Frequency (GHz)	DB(NF())	DB(|S(2,1)|)
0.3	5.19	3.54
0.35	3.31	9.96
0.4	**2.61**	**12.25**
0.45	**2.45**	**11.98**
0.5	2.50	11.04
0.55	2.62	10.09
0.6	2.74	9.28
0.65	2.87	8.61
0.7	2.98	8.06
0.75	3.09	7.60
0.8	3.19	7.21
0.85	3.27	6.88
0.9	3.34	6.59
0.95	3.41	6.33
1	3.47	6.10

Figure 44 shows the full schematic of ARL23M425. A simulation of the transmit chain including the BPSK modulator, power amplifier, and TR switch is shown in figure 45. The receive chain simulation including the low noise amplifier and TR switch is shown in figure 46. Performance of the transmit and receive modes of ARL23M425 are shown in tables 11, 12, and 13. Output power and efficiency are shown at both 2.7 and 3.6 V. The results shown at 2.7 V, should be slightly better using the expected 2.8-V supply. As expected the output power, efficiency, and noise figure are slightly degraded by the insertion loss of the TR switch.

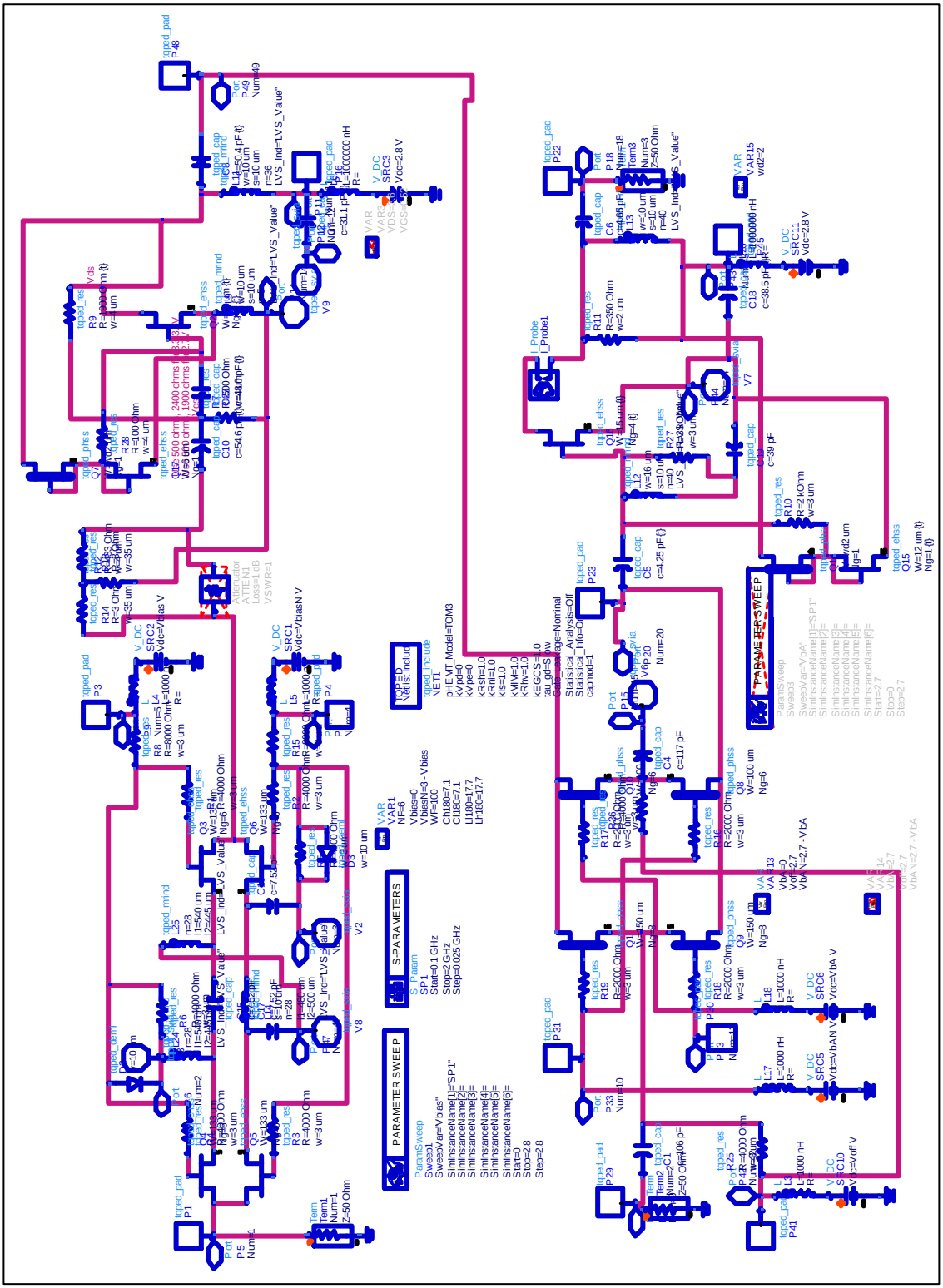

Figure 44. Schematic of ARL23M425, 50 mW 2.8/3.6 V (ADS).

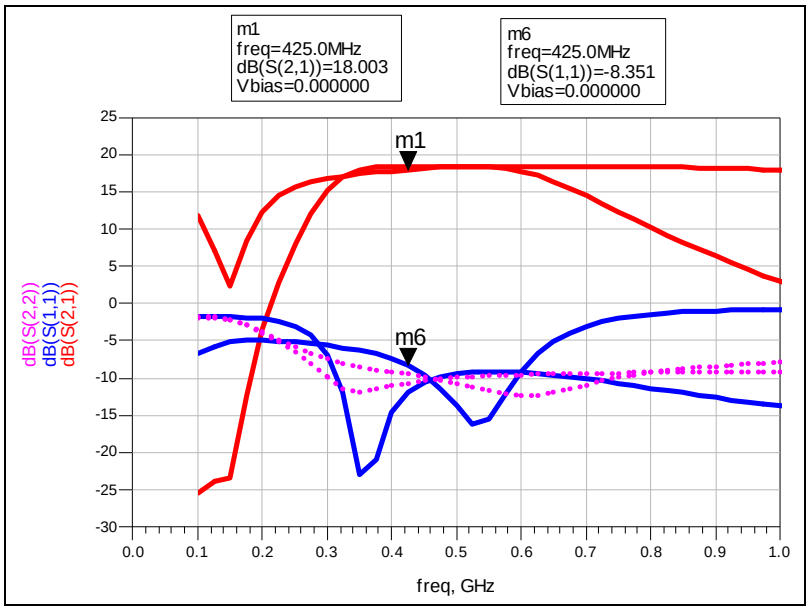

Figure 45. S-parameter simulation of ARL23M425 transmit (ADS).

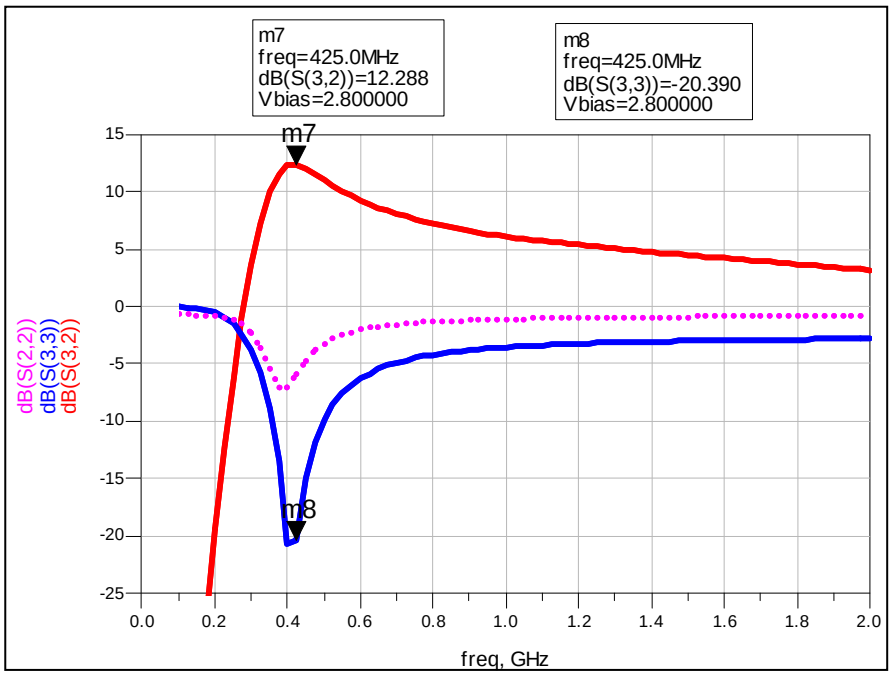

Figure 46. S-parameter simulation of ARL23M425 receive (ADS).

Table 11. Simulated performance of transmit chain for ARL23M425 (2.7 V).

Power (dBm)	Pout 0.425 GHz	PAE 0.425 GHz	Gain 0.425 GHz
–16	1.99	1.62	17.99
–14	3.98	2.57	17.98
–12	5.96	4.05	17.96
–10	7.93	6.39	17.93
–8	9.87	10.02	17.87
–6	11.71	15.63	17.71
–4	13.31	23.93	17.31
–2	14.41	33.61	16.41
0	**14.78**	**39.55**	**14.78**
2	14.74	41.75	12.74

Table 12. Simulated performance of transmit chain for ARL23M425 (3.6 V).

Power (dBm)	Pout 0.425 GHz	PAE 0.425 GHz	Gain 0.425 GHz
–16	1.99	1.12	17.99
–14	3.98	1.76	17.98
–12	5.97	2.79	17.97
–10	7.95	4.40	17.95
–8	9.92	6.92	17.92
–6	11.86	10.81	17.86
–4	13.74	16.73	17.74
–2	15.42	25.14	17.42
0	**16.41**	**33.61**	**16.41**
2	16.69	38.15	14.69

Table 13. Simulated performance of receive chain for ARL23M425.

Frequency (GHz)	DB(NF())	DB(|S(2,1)|)
0.3	5.17	3.54
0.35	3.28	9.96
0.4	**2.58**	**12.25**
0.45	**2.43**	**11.98**
0.5	2.48	11.04
0.55	2.59	10.09
0.6	2.72	9.28
0.65	2.85	8.61
0.7	2.96	8.06
0.75	3.06	7.60
0.8	3.15	7.21
0.85	3.24	6.88
0.9	3.31	6.58
0.95	3.38	6.33
1	3.45	6.10

Figure 47 shows the full schematic of ARL24DB. A simulation of the transmit chain including the BPSK modulator, power amplifier, and TR switch is shown in figure 48. The receive chain simulation including the low noise amplifier and TR switch is shown in figure 49. Performance of the transmit and receive modes of ARL24DB are shown in tables 14 through 18. Output power and efficiency are shown for the frequencies 425 and 900 MHz as well as supply voltages of 2.7 and 3.6 V. As expected the output power, efficiency, and noise figure are slightly degraded by the insertion loss of the TR switch.

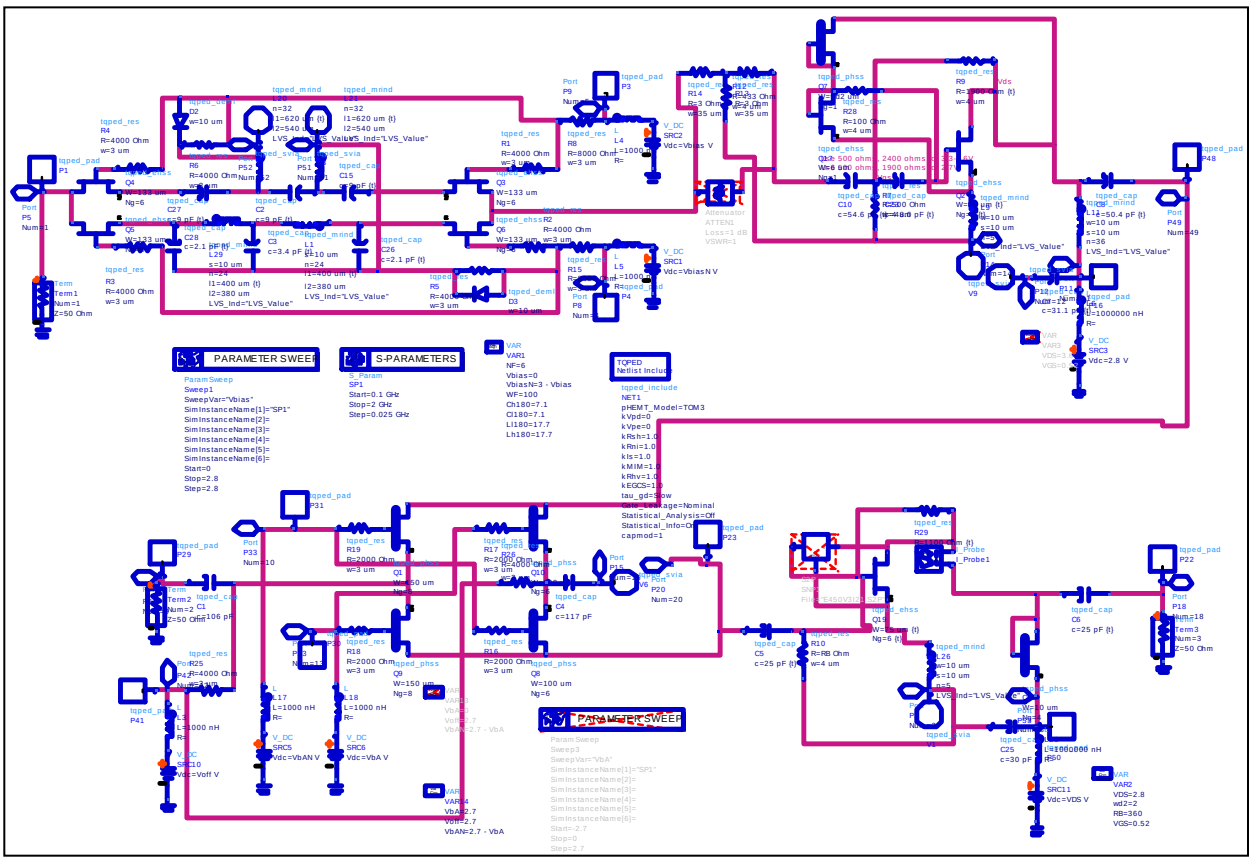

Figure 47. Schematic of ARL24DB, 425/900 MHz and 2.8/3.6 V (ADS).

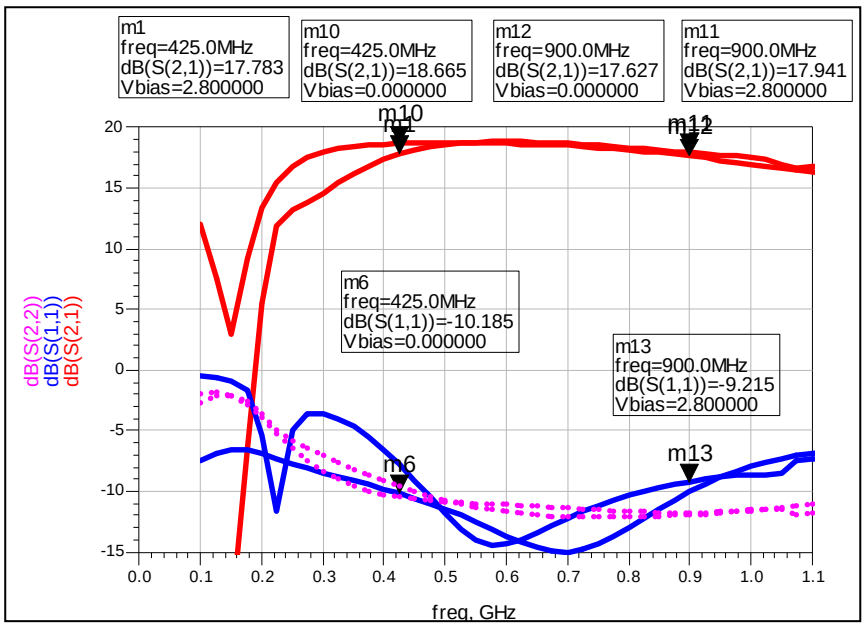

Figure 48. S-parameter simulation of ARL24DB transmit (ADS).

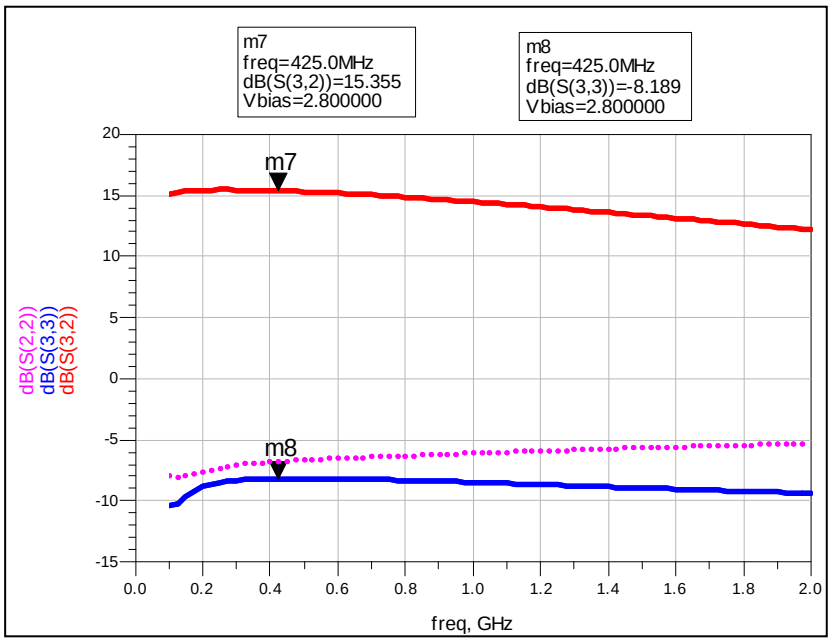

Figure 49. S-parameter simulation of ARL24DB receive (ADS).

Table 14. Simulated performance of transmit chain for ARL24DB (425 M/2.7 V).

Power (dBm)	Pout 0.425 GHz	PAE 0.425 GHz	Gain 0.425 GHz
–16	2.58	1.86	18.58
–14	4.57	2.94	18.57
–12	6.55	4.65	18.55
–10	8.51	7.31	18.51
–8	10.43	11.44	18.43
–6	12.22	17.75	18.22
–4	13.71	26.63	17.71
–2	14.58	35.08	16.58
0	**14.83**	**39.66**	**14.83**
2	14.74	41.21	12.74

Table 15. Simulated performance of transmit chain for ARL24DB (425 M/3.6 V).

Power (dBm)	Pout 0.425 GHz	PAE 0.425 GHz	Gain 0.425 GHz
–16	2.57	1.28	18.57
–14	4.56	2.02	18.56
–12	6.55	3.19	18.55
–10	8.53	5.03	18.53
–8	10.49	7.89	18.49
–6	12.41	12.30	18.41
–4	14.25	18.87	18.25
–2	15.76	27.44	17.76
0	**16.50**	**34.24**	**16.50**
2	16.73	37.94	14.73

Table 16. Simulated performance of transmit chain for ARL24DB (900 M/2.7 V).

Power (dBm)	Pout 0.90 GHz	PAE 0.90 GHz	Gain 0.90 GHz
–16	1.63	1.49	17.63
–14	3.63	2.36	17.63
–12	5.61	3.74	17.61
–10	7.59	5.90	17.59
–8	9.55	9.28	17.55
–6	11.45	14.56	17.45
–4	13.17	22.68	17.17
–2	14.50	33.46	16.50
0	**15.06**	**40.93**	**15.06**
2	15.16	44.03	13.16

Table 17. Simulated performance of transmit chain for ARL24DB (900 M/3.6 V).

Power (dBm)	Pout 0.90 GHz	PAE 0.90 GHz	Gain 0.90 GHz
–16	1.58	1.02	17.58
–14	3.58	1.61	17.58
–12	5.57	2.54	17.57
–10	7.56	4.01	17.56
–8	9.54	6.33	17.54
–6	11.50	9.94	17.50
–4	13.43	15.50	17.43
–2	15.24	23.81	17.24
0	**16.54**	**33.79**	**16.54**
2	17.00	39.59	15.00

Table 18. Simulated performance of receive chain for ARL24DB.

Frequency (GHz)	DB(NF())	DB(|S(2,1)|)
0.3	2.31	15.44
0.35	2.25	15.41
0.4	**2.21**	**15.38**
0.45	**2.19**	**15.33**
0.5	2.18	15.28
0.55	2.17	15.22
0.6	2.16	15.15
0.65	2.16	15.08
0.7	2.16	15.01
0.75	2.16	14.93
0.8	2.16	14.84
0.85	2.17	14.75
0.9	**2.17**	**14.66**
0.95	2.18	14.56
1	2.19	14.46

The circuits that make up the full RFIC were initially simulated with MWO. They were later simulated with ADS with similar results. Most of these subcircuits were included on the test chip ARL25, so those individual layouts were simulated with Sonnet's 2.5-D Simulator. This helps to verify the actual layout connections, which are also verified with a layout versus schematic check (see section 7). Also, this checks the layout for unsimulated coupling, which caused a stability issue with the 2.4-GHz low noise amplifier from the 1st pass designs. Since ADS and MWO do not simulate the full coupling of the actual layout, only the Sonnet EM simulator showed an indication of the stability problem that occurred in that particular amplifier design. The Sonnet EM simulations assumes lossless 2-D metallization to reduce simulation times, so the losses will be underestimated, but unsimulated coupling and parasitics will be included. Results of the Sonnet simulations of the individual 50-mW power amplifier, 100-mW power

amplifier, 425-MHz low noise amplifier, and the 425-MHz BPSK modulator agreed well with the ADS and MWO simulations.

Test chip ARL25 contains a copy of the narrowband 425-MHz low noise amplifier included on the first three designs. The simulation results using ADS are similar to MWO with a slight increase in the noise figure (figures 50, 51, and 52). Sonnet was used to simulate the actual layout (figure 53) to check for any unsimulated parasitics. The three PHEMT connections are simulated as internal ports, and then the S-parameter file created for the Sonnet simulation is combined with the PHEMTs in ADS (or MWO) for comparison to the original simulations. Figures 54 and 55 show good agreement between the original simulations and the Sonnet simulations of the actual physical layout. Since the Sonnet EM simulation used lossless 2-D metal, the low noise amplifier gain tends to be slightly higher and the noise figure slightly lower, but overall agrees very well with the linear ADS/MWO simulations.

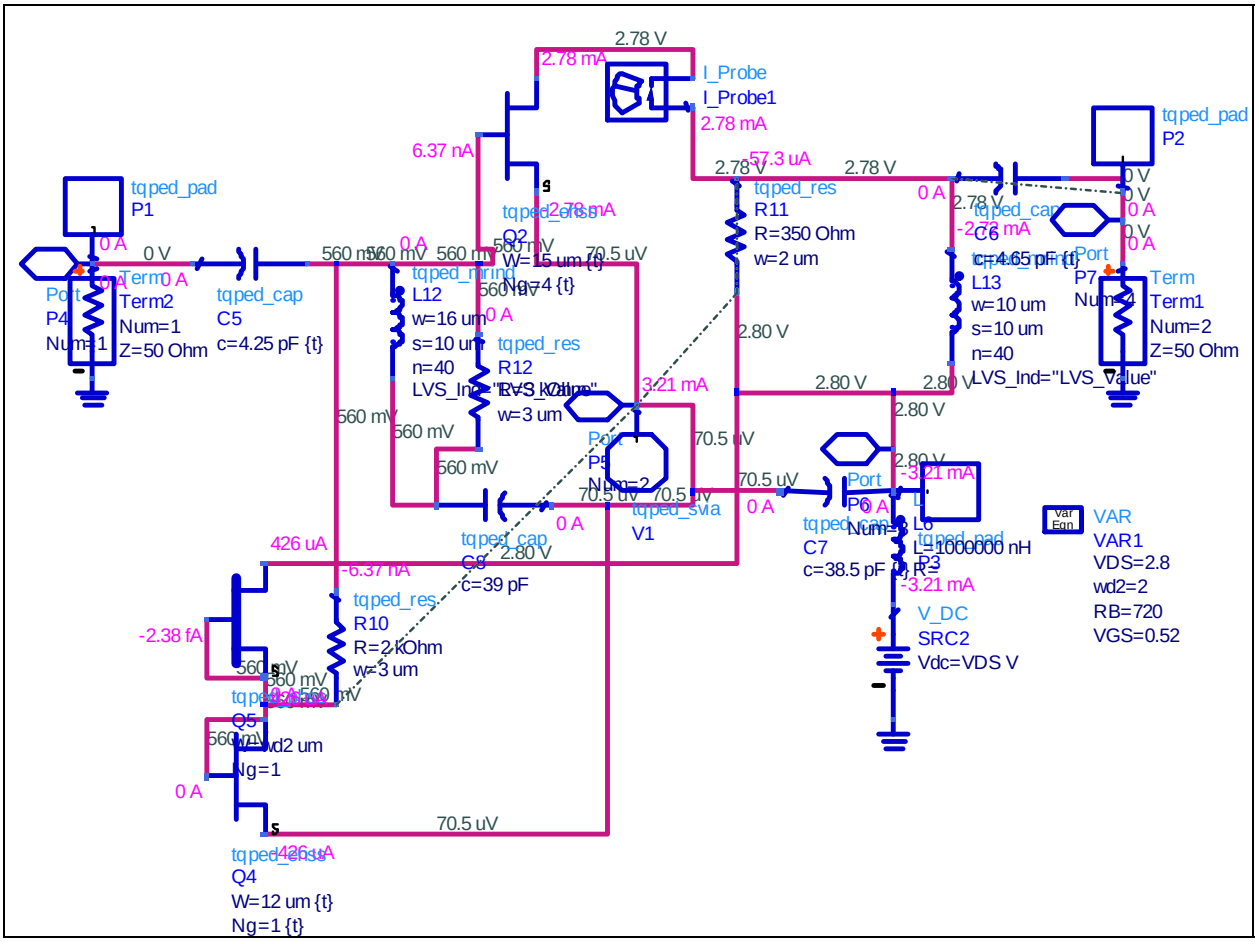

Figure 50. Schematic of the 425-MHz low noise amplifier, ARL25 (ADS).

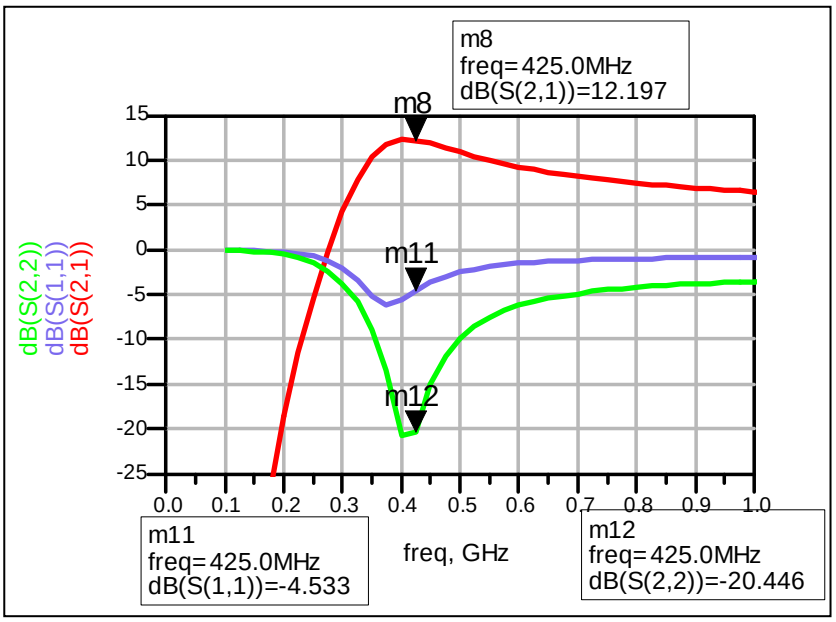

Figure 51. S-parameter simulation of the 425-MHz low noise amplifier, ARL25 (ADS).

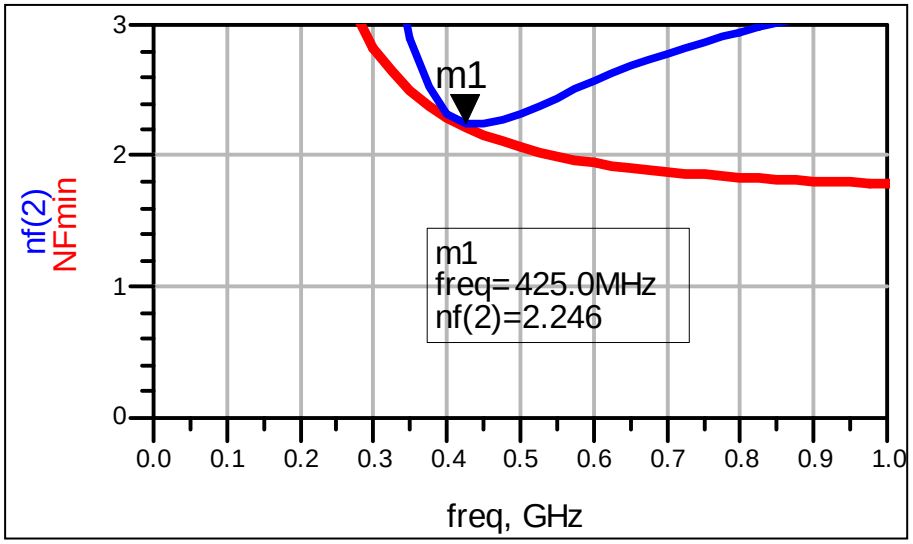

Figure 52. Noise figure simulation of the 425-MHz low noise amplifier, ARL25 (ADS).

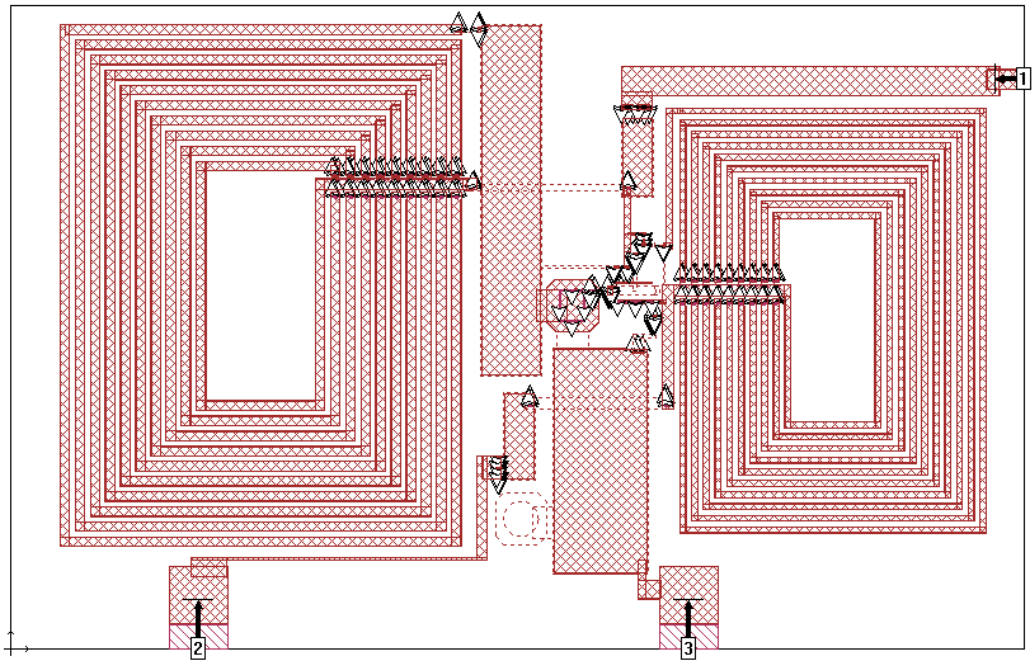

Figure 53. Sonnet EM layout simulation of the 425-MHz low noise amplifier, ARL25 (ADS).

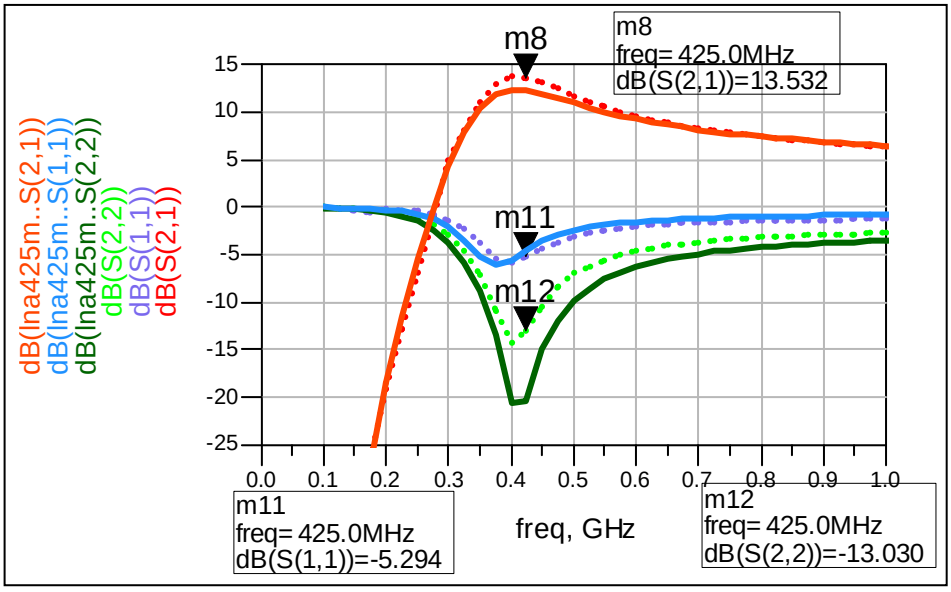

Figure 54. Sonnet (dotted) vs. ADS S-parameter simulation of the 425-MHz low noise amplifier, ARL25.

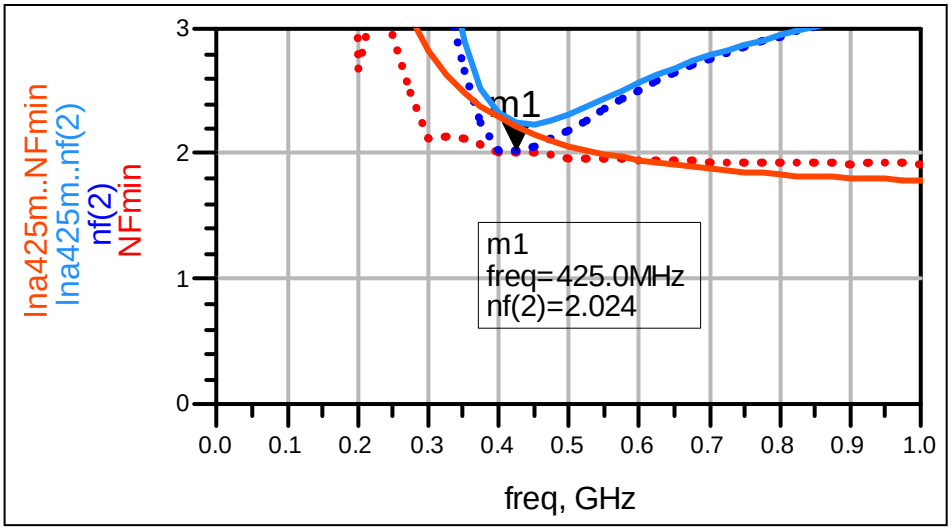

Figure 55. Sonnet (dotted) vs. ADS noise figure simulation of the 425-MHz low noise amplifier, ARL25.

A broadband low noise amplifier design that worked well from the 1st pass designs was slightly modified to reduce the current consumption. Modifying the feedback and stabilizing resistors to 1100 and 360 ohms as well as reducing the size of the active load PHEMT from a 4x15 to 4x10 µm, reduced the current consumption of the low noise amplifier, while still providing sufficient broadband gain and good performance. Figures 56, 57, and 58 show the ADS schematic and simulations of the modified broadband amplifier used in ARL24DB. This low noise amplifier subcircuit is included as a probe-able test circuit at the bottom center of the layout.

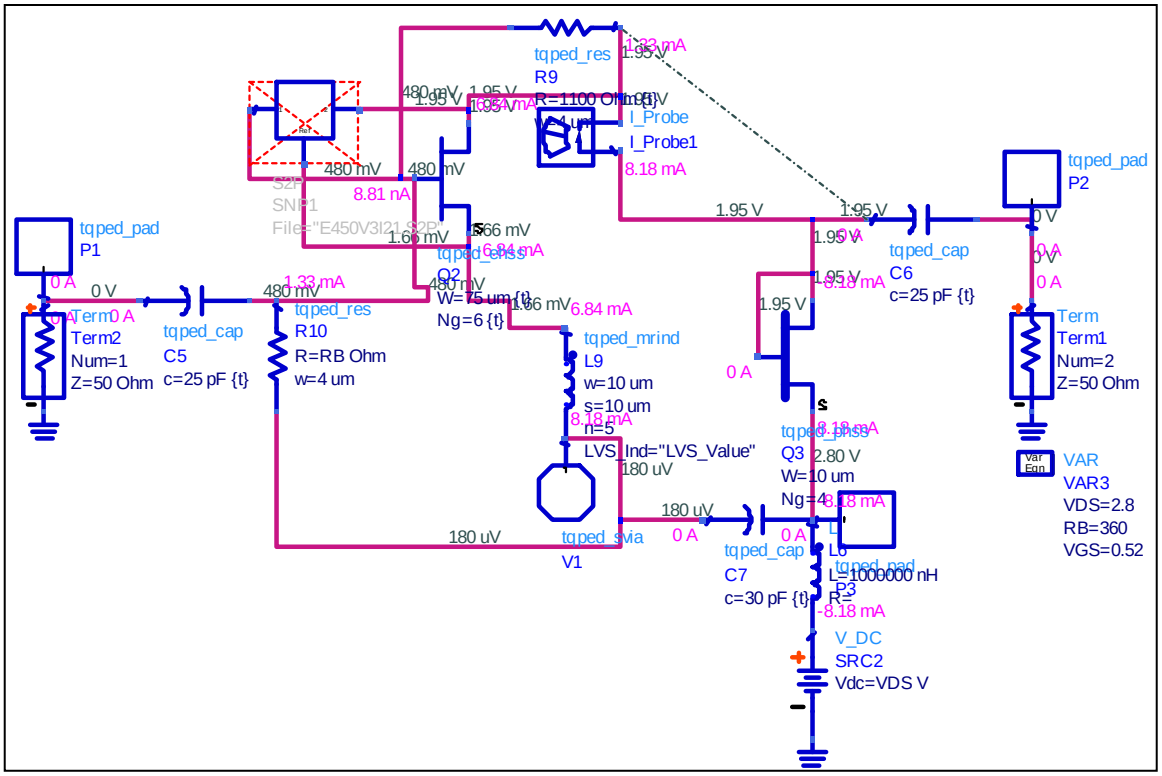

Figure 56. Schematic of the modified (8 mA) broadband low noise amplifier, ARL24DB (ADS).

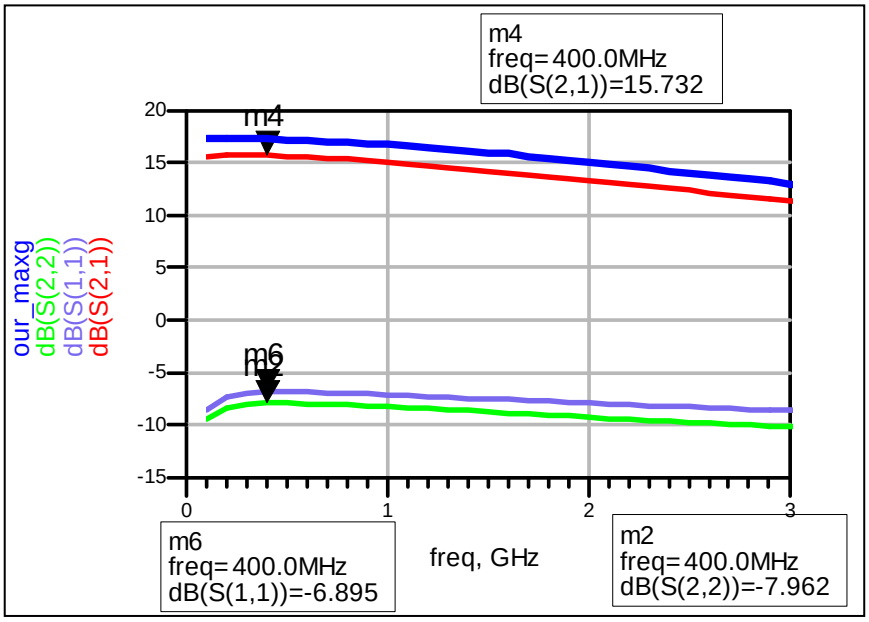

Figure 57. Simulation of the modified (8 mA) broadband low noise amplifier, ARL24DB (ADS).

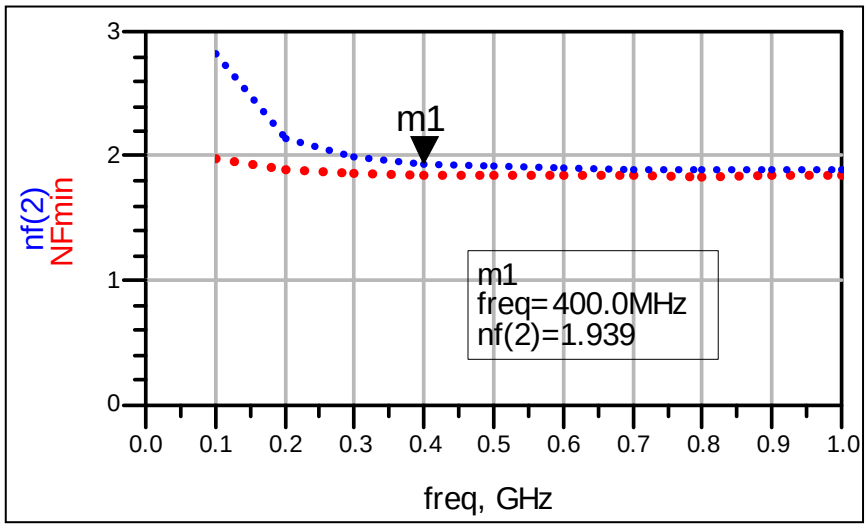

Figure 58. NF simulation of the modified (8 mA) broadband low noise amplifier, ARL24DB (ADS).

Test chip ARL25 contains a copy of the narrowband 425 MHz 100 mW PA included on the first design (ARL21M425). The simulation results using ADS are similar to MWO (see figures 59, 60, and 61). Sonnet was used to simulate the physical layout (figure 62) to check for any unsimulated parasitics. The three PHEMT connections are simulated as internal ports, and then the S-parameter file created for the sonnet simulation is combined with the PHEMTs in ADS (or MWO) for comparison to the original simulations. Figure 63 shows good agreement between the original simulation and the Sonnet simulation of the physical layout.

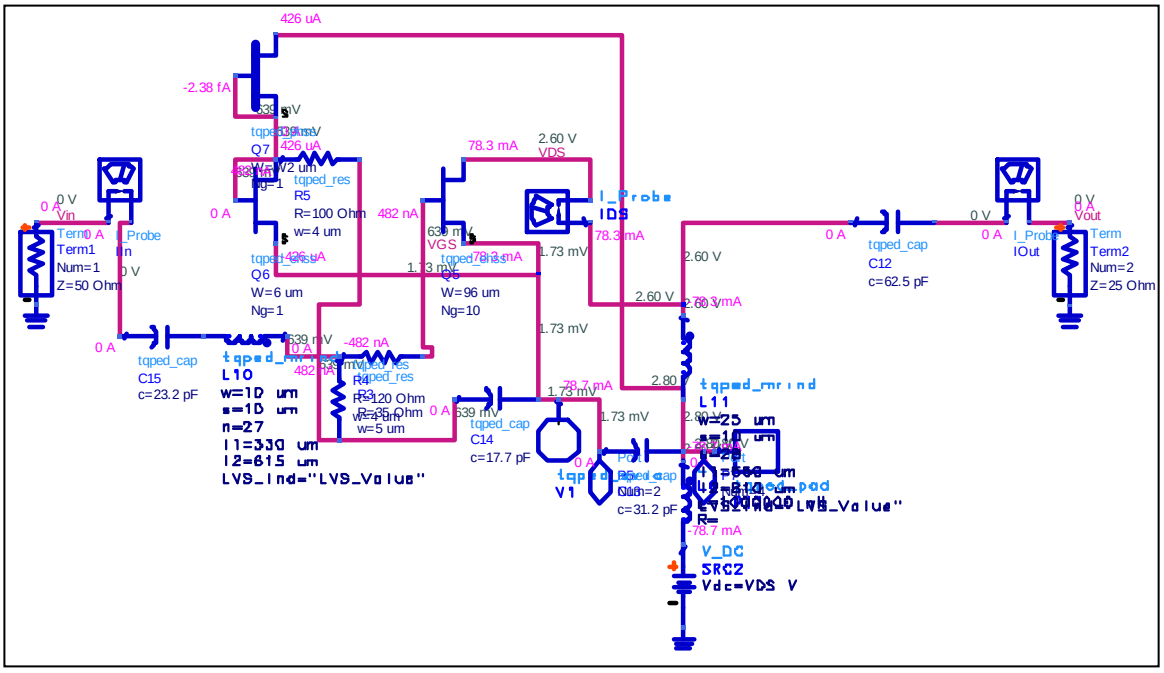

Figure 59. Schematic of the 425-MHz, 100-mW power amplifier, ARL25 (ADS).

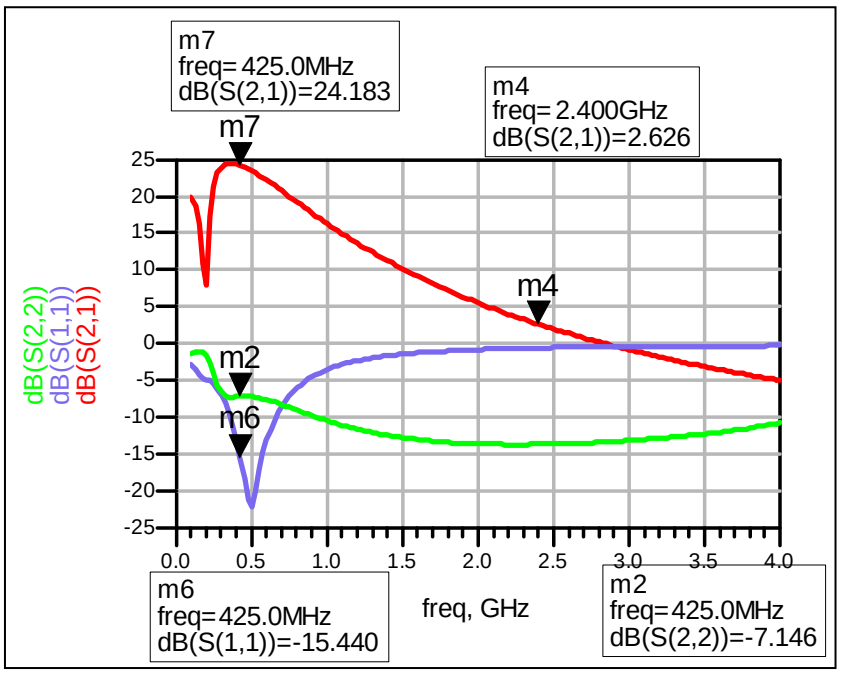

Figure 60. Simulation of the 425-MHz, 100-mW power amplifier, ARL25 (ADS).

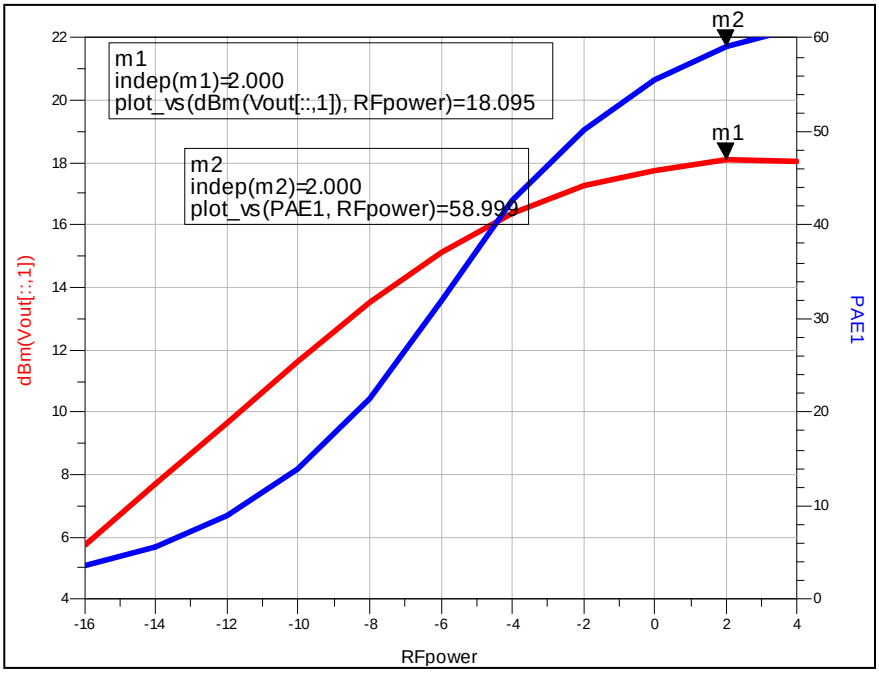

Figure 61. Power simulation of the 425-MHz, 100-mW power amplifier, ARL25 (ADS).

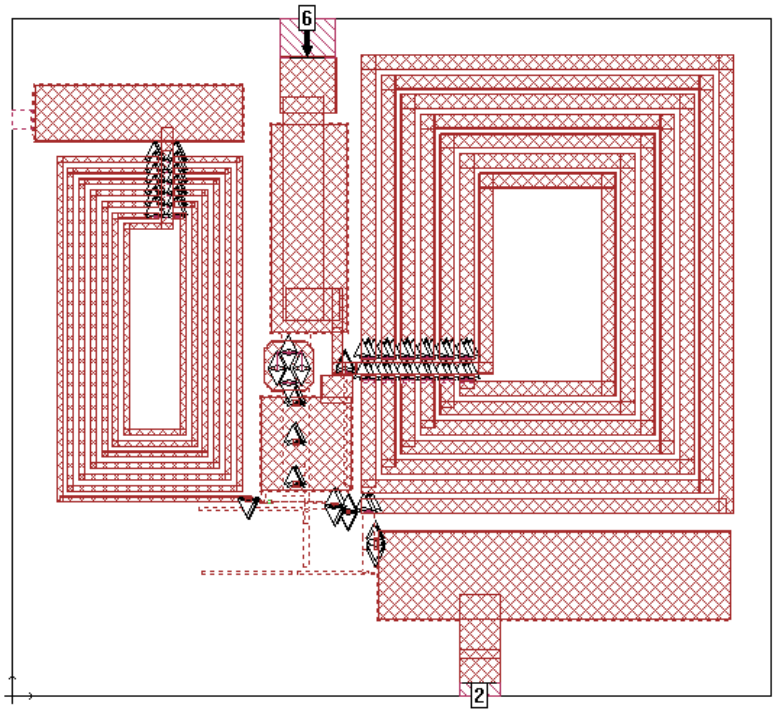

Figure 62. Sonnet EM layout simulation of the 425-MHz, 100-mW power amplifier, ARL25 (ADS).

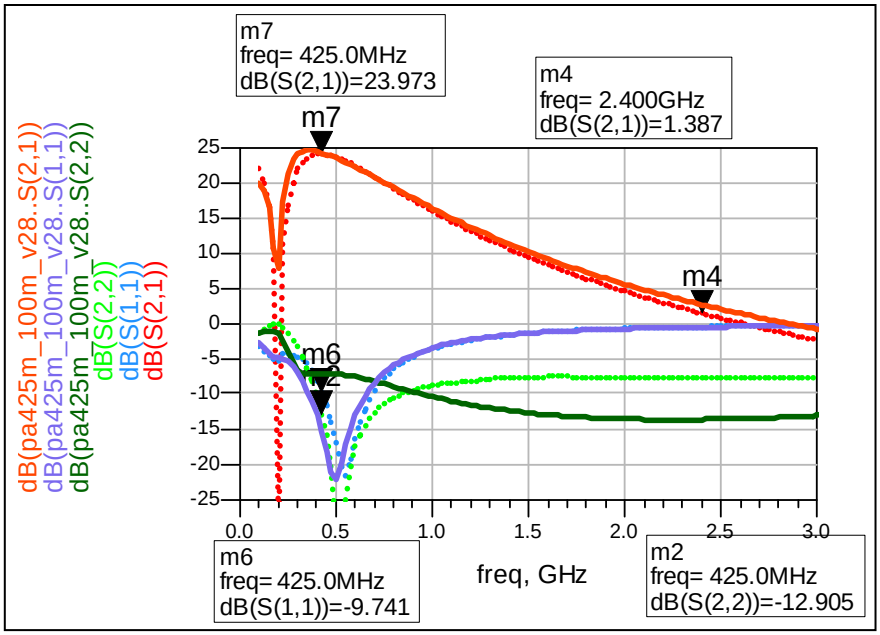

Figure 63. Sonnet (dotted) vs. ADS S-parameter simulation of the narrowband 100-mW power amplifier, ARL25.

A copy of the narrowband 425-MHz, 50-mW power amplifier from the second design (ARL22M425) is also included on test chip ARL25. The simulation results using ADS are similar to MWO (figures 64, 65, and 66). Sonnet was used to simulate the physical layout (figure 67) to check for any unsimulated parasitics. The three PHEMT connections are simulated as internal ports, and then the S-parameter file created for the sonnet simulation is combined with the PHEMTs in ADS (or MWO) for comparison to the original simulations. Figure 68 shows good agreement between the original simulation and the Sonnet simulation of the physical layout.

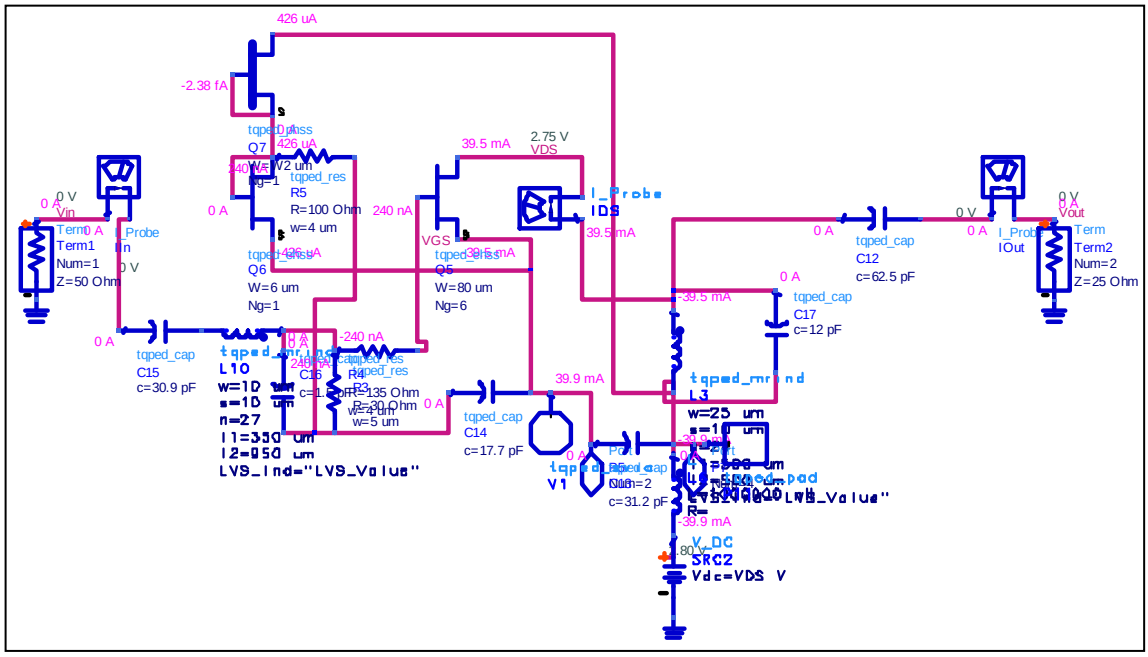

Figure 64. Schematic of the 425-MHz, 50-mW power amplifier, ARL25 (ADS).

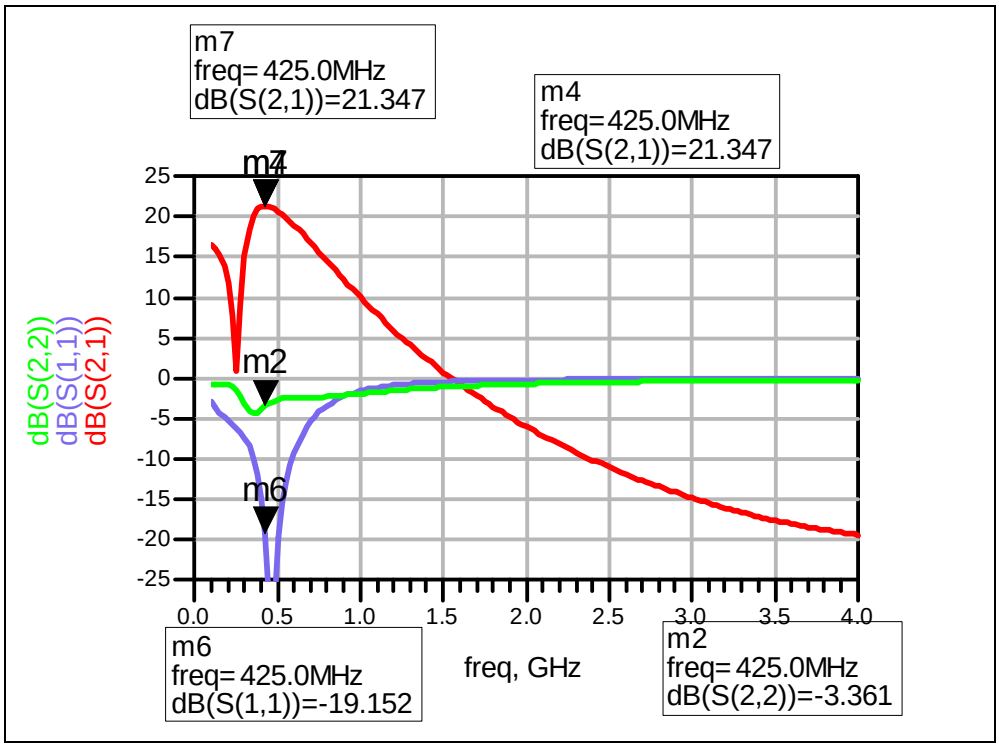

Figure 65. Simulation of the 425-MHz, 50-mW power amplifier, ARL25 (ADS).

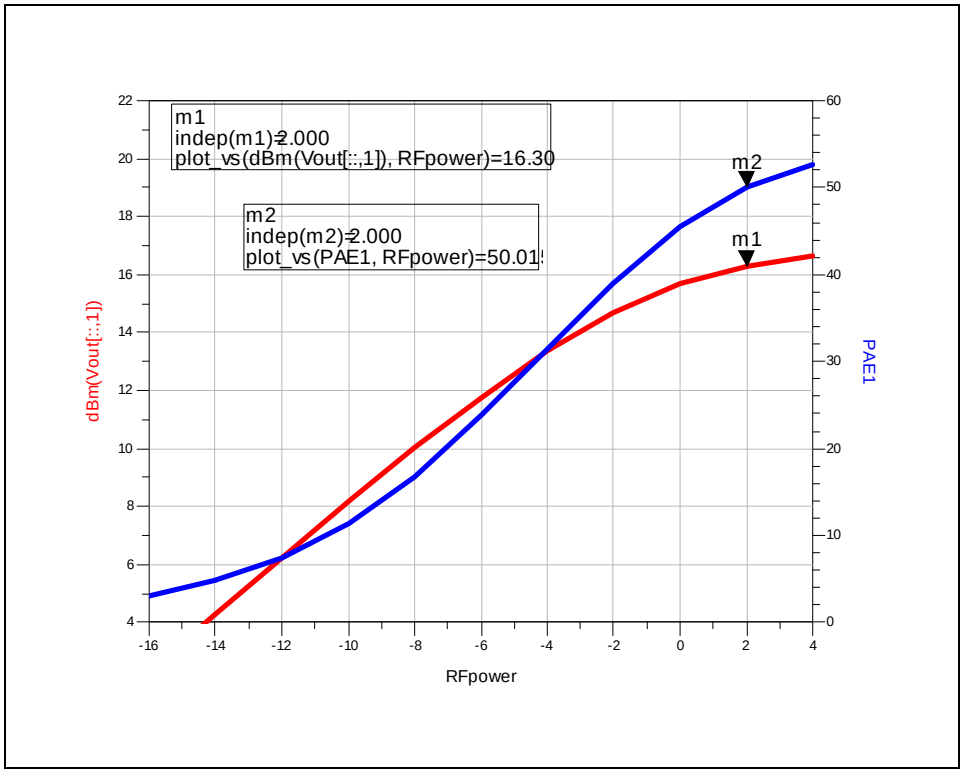

Figure 66. Power simulation of the 425-MHz, 50-mW power amplifier, ARL25 (ADS).

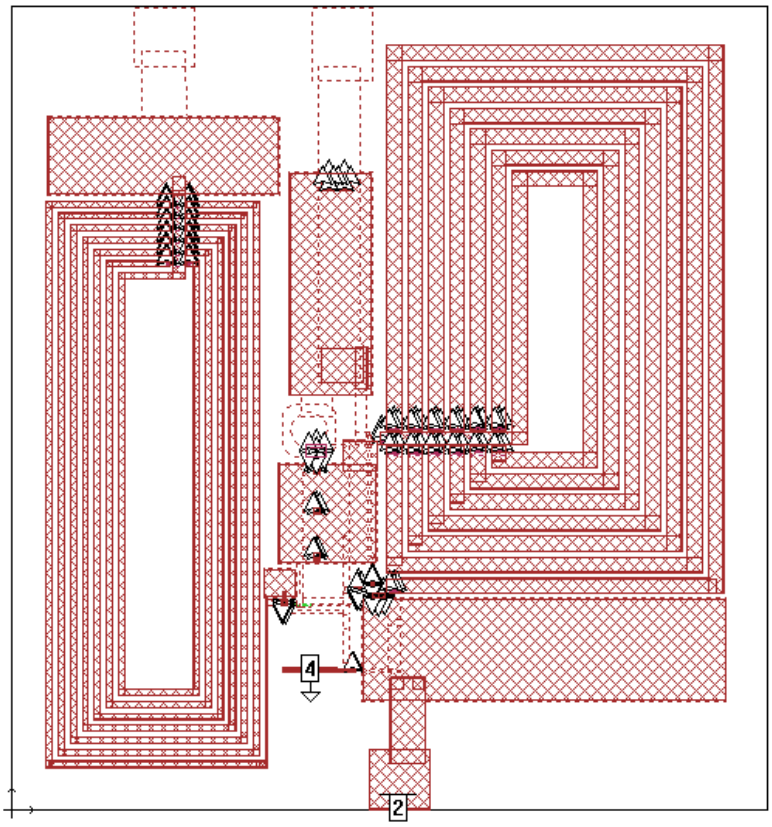

Figure 67. Sonnet EM layout simulation of the 425-MHz, 50-mW power amplifier, ARL25 (ADS).

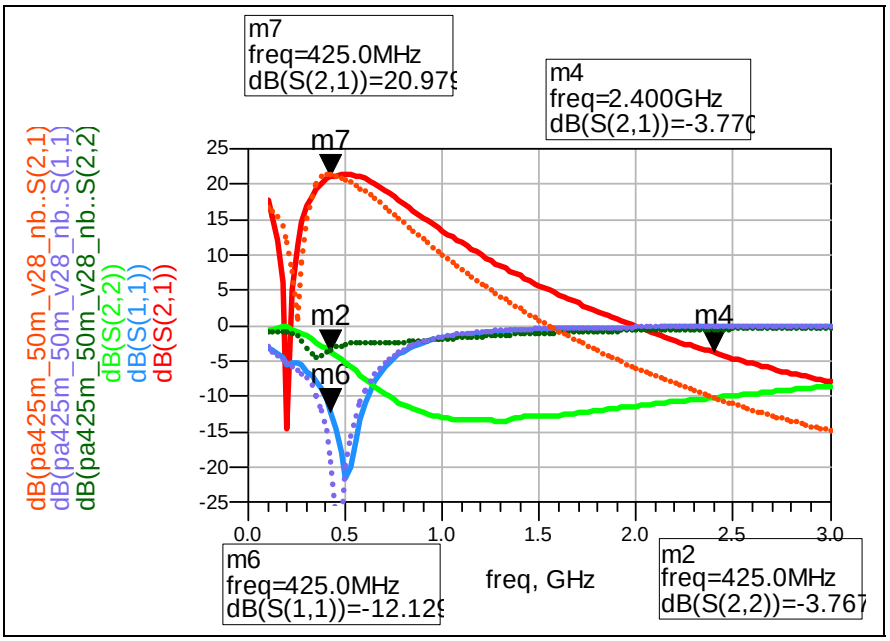

Figure 68. Sonnet (dotted) vs. ADS S-parameter simulation of the narrowband 50-mW power amplifier, ARL25

The TR switch design that worked well from the 1st pass design, but had higher than desired insertion loss, was modified for the 2nd pass to reduce the insertion loss to an expected 0.5 dB while retaining the positive control logic. ADS was used to re-simulate the TR switch (figure 69 shows the schematic) and the simulations are similar to that obtained with MWO (figure 70).

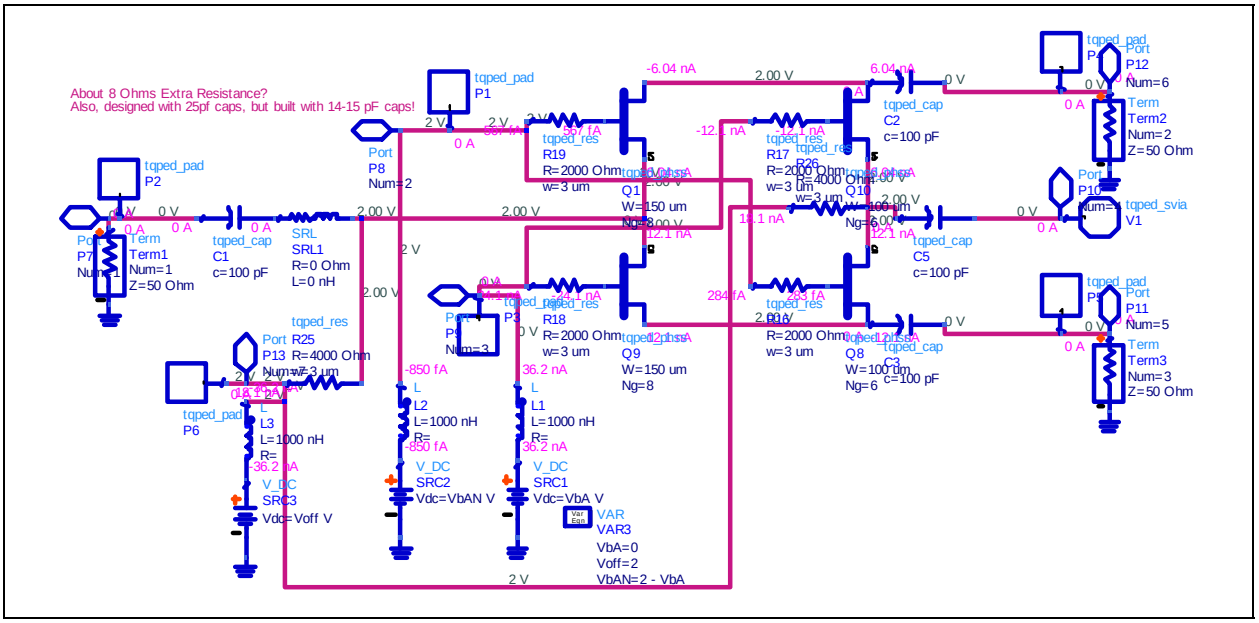

Figure 69. Schematic of the TR switch, ARL25 (ADS)

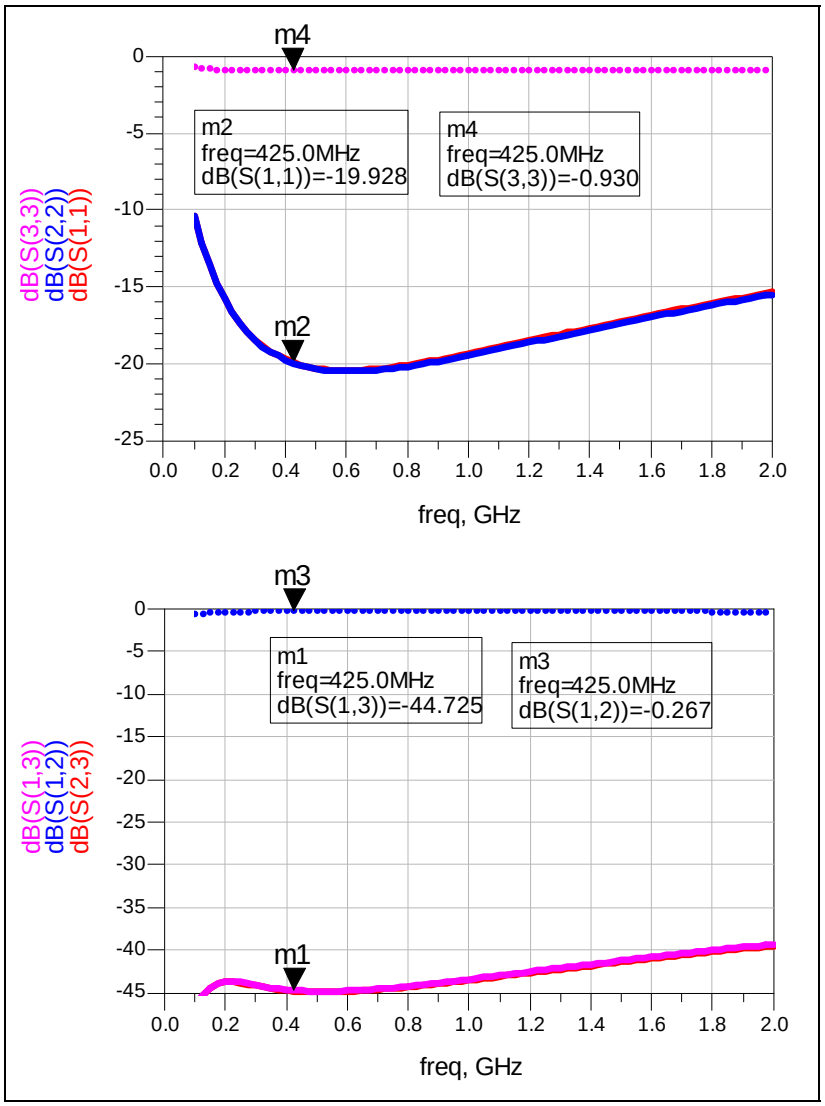

Figure 70. Simulation of the TR switch, ARL25 (ADS)

The BPSK modulators, both the narrowband 425-MHz and the dual 425/900-MHz designs were not included as standalone test circuits. A narrowband version was very slightly retuned from the original 1st pass design to shift the center frequency from 450 to 425 MHz. The dual 425/ 900-MHz modulator adds two more elements to the high pass and low pass filters to provide a broadband 180° phase shift. The topology of low pass filter was reduced to two series inductors rather than three to save space. Only the narrowband modulator was simulated with Sonnet for comparison to ADS. The schematic and simulation results for the 425-MHz BPSK modulator using ADS are shown in figures 71, 72, and 73. Sonnet was used to simulate the physical layout (figure 74) to check for any unsimulated parasitics. The four switching PHEMTs were not part of the Sonnet EM simulation. For comparison, the S-parameter file created for the layout using Sonnet is combined with the PHEMT switches in ADS (or MWO) with good agreement to the original simulations. Figures 75 and 76 show good agreement between the original simulations

and using Sonnet to simulate the physical layout. Since the Sonnet EM simulation used lossless 2-D metal, the modulator insertion loss tends to be underestimated, but otherwise agrees very well with the linear ADS/MWO simulations.

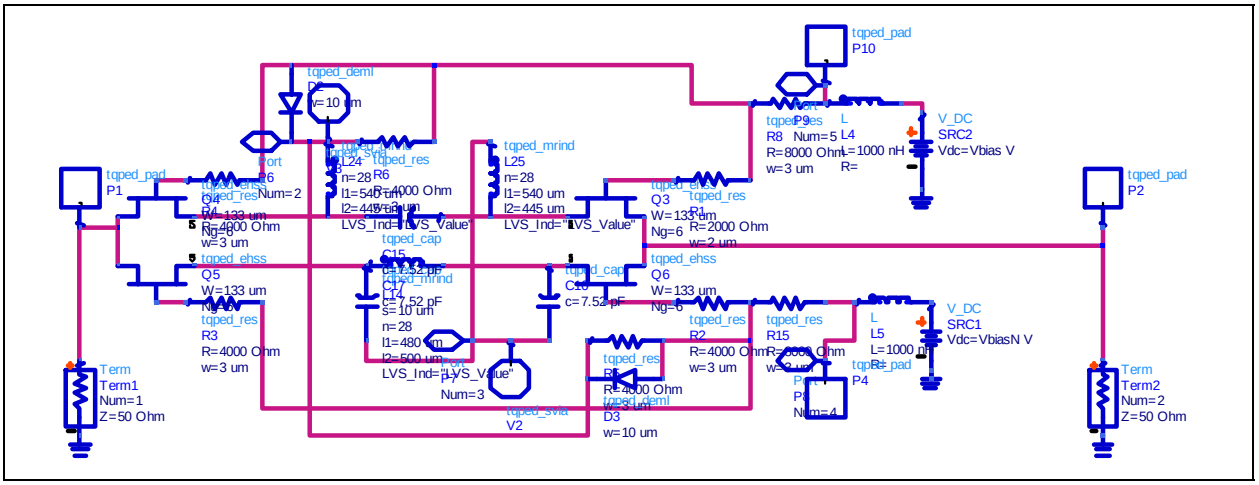

Figure 71. Schematic of the 425-MHz BPSK modulator (ADS).

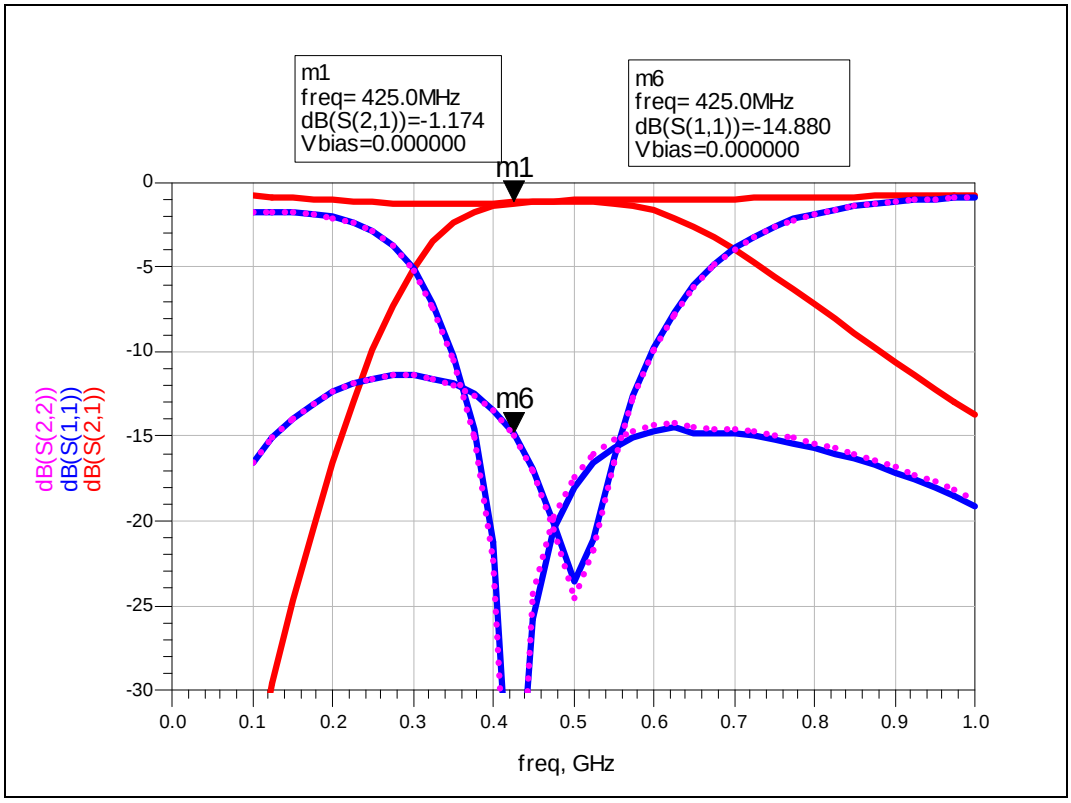

Figure 72. Insertion loss simulation of the 425-MHz BPSK modulator (ADS).

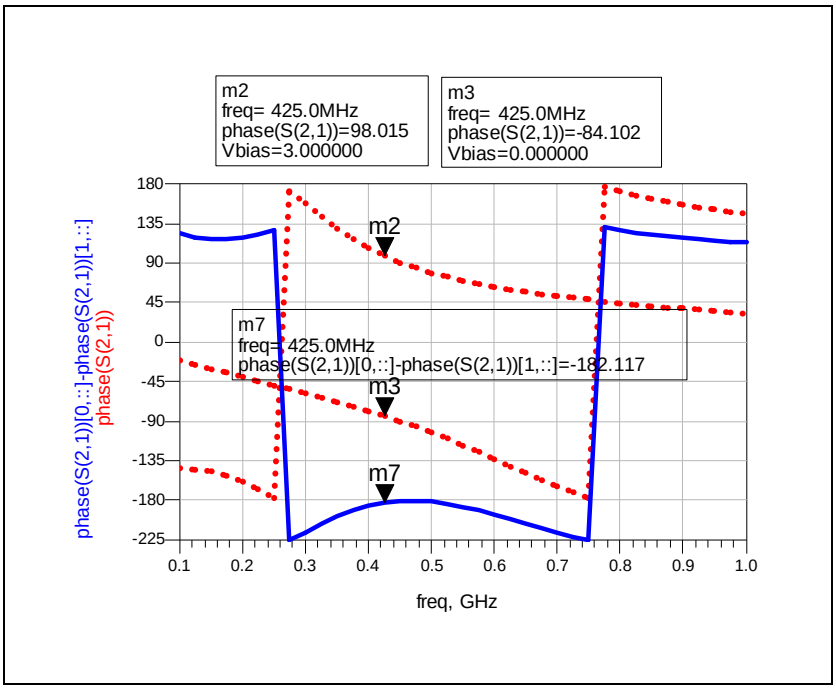

Figure 73. Phase simulation of the 425-MHz BPSK modulator (ADS).

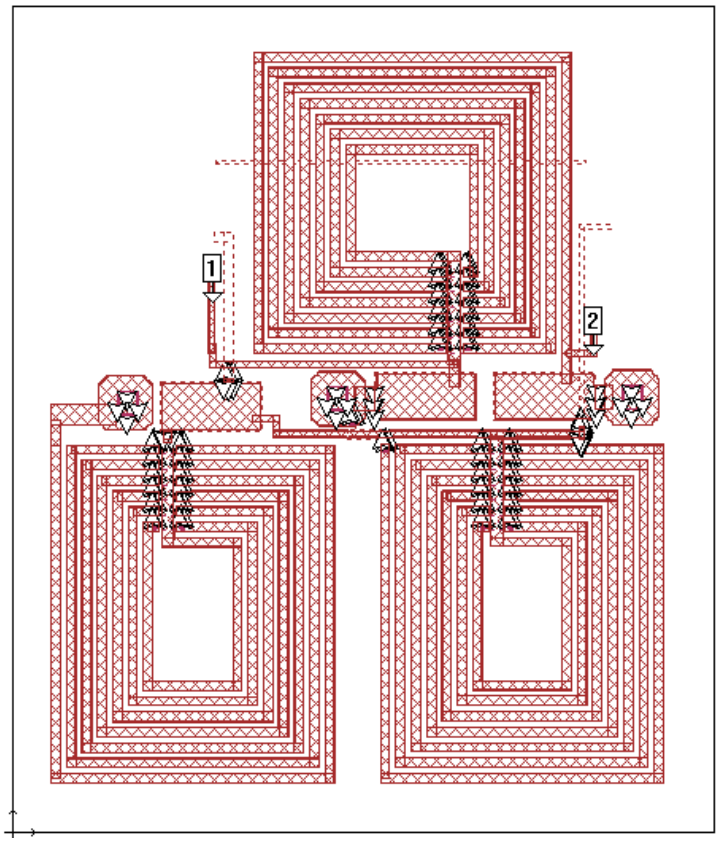

Figure 74. Sonnet EM layout simulation of the 425-MHz BPSK modulator.

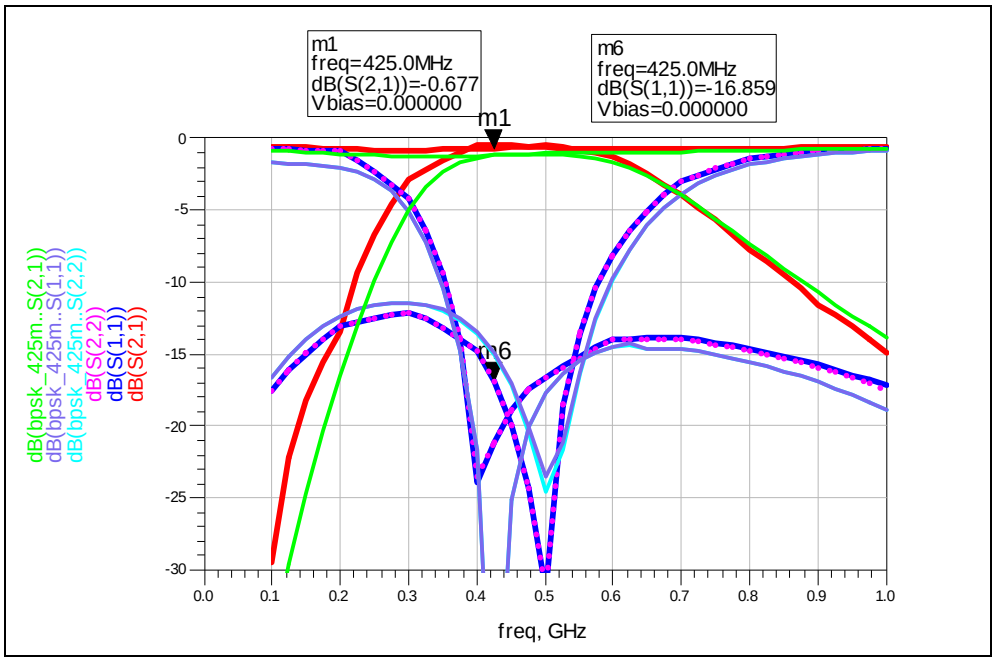

Figure 75. Sonnet (dotted) vs. ADS S-parameter simulation of the narrowband BPSK modulator.

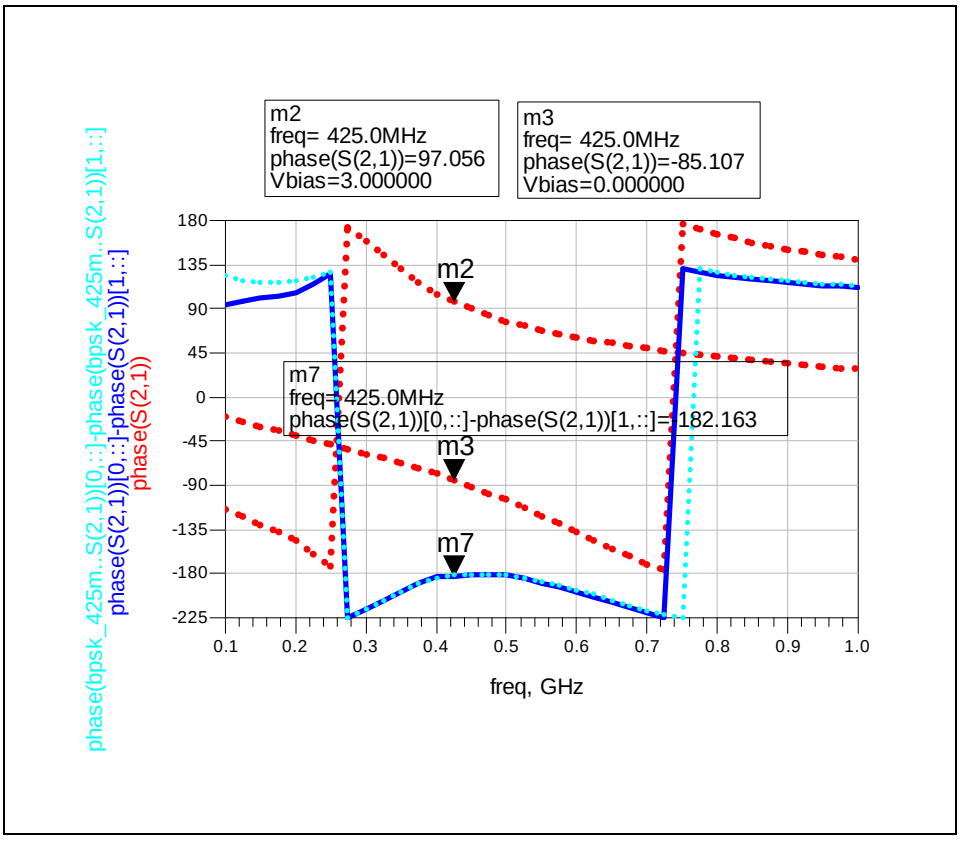

Figure 76. Sonnet (dotted) vs. ADS phase simulation of narrowband BPSK modulator.

5. Integration of RFIC Matching Circuits

Most RFIC transceivers require quite a few external matching elements. Not only do these elements take up board space in the system, but they also tend to narrow the operation to a specific frequency band. For instance the Texas Instruments (TI) CC1000 sub-1 GHz transceiver and the more recent TI CC1100 sub-1 GHz transceiver were of interest for targeting a combined RFIC with the booster IC. While the transceiver may theoretically operate over several bands, the RFIC manufacturers expect the system to include all of the matching elements external to their RFIC. Multiple matching circuits are recommended depending on which band is desired. It would be difficult to broadband the matching circuits required by the RFIC. Also, it would save considerable board space if the matching circuits and balun circuits for the various RFIC transceivers could be integrated into a single small IC or package. A broadband or dual band antenna will be needed for the system, but we do not discuss that issue here. A small compact efficient system would include the RFIC, a small packaged IC incorporating all of the matching/balun elements, and the active booster IC to improve the RF performance for enhanced operating range or bandwidth. Figure 77 illustrates the concept of integrating the typical matching elements required between the RFIC and the antenna. The antenna connection in the figure can easily be extended to a booster IC plus the antenna for enhanced performance.

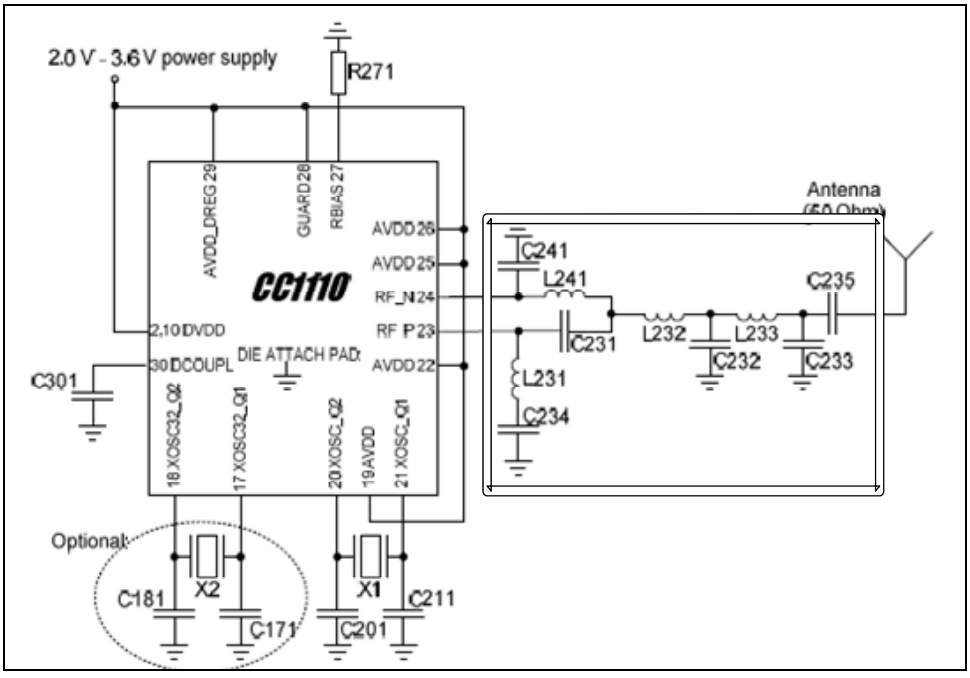

Figure 77. Concept of integrating RFIC matching elements into an IC for size, weight, and power (SWAP).

To demonstrate the integration of matching elements for improved SWAP, the data sheets for the CC1000 and CC1100 were used for initial designs of an integrated matching circuit. These two designs illustrate some of the difficulties and pitfalls of designing and integrating these matching circuits required by the RFIC. The older CC1000 design has a separate single ended RF input and RF output but the recommended matching circuit combines these two connections to a single antenna connection. It is not clear from the data sheet what the affect of this internal TR switch has on using the RF input and RF output as separate connections. Also, in attempts to simulate the recommended matching circuits and match to the specified impedances, there seem to be discrepancies for every frequency band. Unfortunately, there were no systems available with these RFICs to take direct measurements of the impedances and discern the best approach for matching. To complicate matters further, the newer design of the CC1100 has a very different set of impedances and recommended matching circuits that are not compatible with the earlier CC1000 RFIC. Likewise the simulations of the recommended CC1100 matching circuits do not seem to match the specified impedances. The CC1100 has the further complication that the RF connections are differential with a single pair of pads for a single RF input/output. Recall that the CC1000 RF connections were separate single ended connections combined into a single matching circuit with the possibility of some unspecified affect from an internal TR switch. At least the CC1100 looks promising in that the impedances recommended seem much closer to the center of a 50-ohm Smith chart, making their use more likely to be tolerant of matching errors and discrepancies. It would appear that the CC1100 is more tolerant of matching circuit variation than the older CC1000. However, there is no RFIC system available to make direct measurements for verifying the data sheets information.

Given the time constraints, the lumped element matching circuits were designed based on the best understanding of the data sheets for the CC1000 and CC1100. The main target was for the 425 MHz operation of each RFIC as well as a dual band matching circuit for the newer CC1100 design which uses switches to operate at either the 425 MHz band or the 900 MHz band. This was intended to be combined with the ARL24DB Booster IC to provide a small wireless system using the CC1100 RFIC, the integrated matching circuit, and the Booster IC for a switchable dual band operation at 425/900 MHz. At the least, the circuits will demonstrate the feasibility of the size advantages of integrating the matching elements for the RFIC into a single packaged IC. TriQuint does offer a high performance GaAs passive fabrication process (TQRLC) which is less expensive and requires fewer processing steps by omitting the active PHEMT devices, extra masks, and processing steps.

The following are descriptions of the passive designs:

- ARL26DB—This dual band design contains a matching circuit plus RF switches to connect the integrated matching circuit for a TI CC1100 RFIC for operation at either 425 or 900 MHz. One side of the design connects to the differential RF connections of the CC1100 RFIC and the other side switches to one of two single ended RF connections,

intended to be either an input to a transmitter/power amplifier and the other an output from a receiver/low noise amplifier. It is a 95x95 mil die.

- ARL27M425—This design contains discrete lumped elements circuits for an integrated match at 425-MHz circuit for a TI CC1000 RFIC. It separates the recommended matching circuit into an RF input and RF output match for separate connections as either an input to a transmitter/power amplifier or an output from a receiver/low noise amplifier rather than a single-ended connection to an antenna. It is a 95x50 mil die.
- ARL28M900—This design contains discrete lumped elements circuits for an integrated match at 900-MHz circuit for a TI CC1000 RFIC. It separates the recommended matching circuit into an RF input and RF output match for separate connections as either an input to a transmitter/power amplifier or an output from a receiver/low noise amplifier rather than a single-ended connection to an antenna. It is similar to ARL27M425 except for the frequency of operation. It is a 95x50 mil die.
- ARL29M425—This single band design contains a matching circuit to connect the integrated matching circuit for a TI CC1100 RFIC for operation at 425 MHz. One side of the design connects to the differential RF connections of the CC1100 RFIC and the other side connects to a single-ended RF connections, intended to be the antenna connection. It is a 95x50 mil die.
- ARL29M425S—This single band design contains a matching circuit to connect the integrated matching circuit for a TI CC1100 RFIC for operation at 425 MHz. One side of the design connects to the differential RF connections of the CC1100 RFIC and the other side connects to RF switches intended for connection to the input of a transmitter/power amplifier or an output from a receiver/low noise amplifier rather than the single-ended connection to an antenna of ARL29M425 which is a similar design. It is a 95x50 mil die.

The circuit designated as ARL26DB is designed for matching the CC1100 at 425 MHz and also 900 MHz, using PHEMT switches to choose between the two frequency bands (figure 78). The values of the lumped elements and the topologies of the matching circuits used are the ones recommended in the CC1100 data sheet Connections to the CC1100 on the upper-left and lower-left sides of the layout use a differential RF connection while the right-hand side of the layout has switches with a separate control to select between one of two RF single-ended connections, presumably the transmit and receive paths of the booster IC. A preliminary wire bond diagram of the die in a 4x4 mm SEMPAC, 20-pin, 4x4 mm QFN package is shown in figure 79. Note that this circuit is mostly passive, i.e., uses lumped matching elements, but also uses PHEMTs as switches to choose the frequency band, and to choose one of two single-ended RF connections.

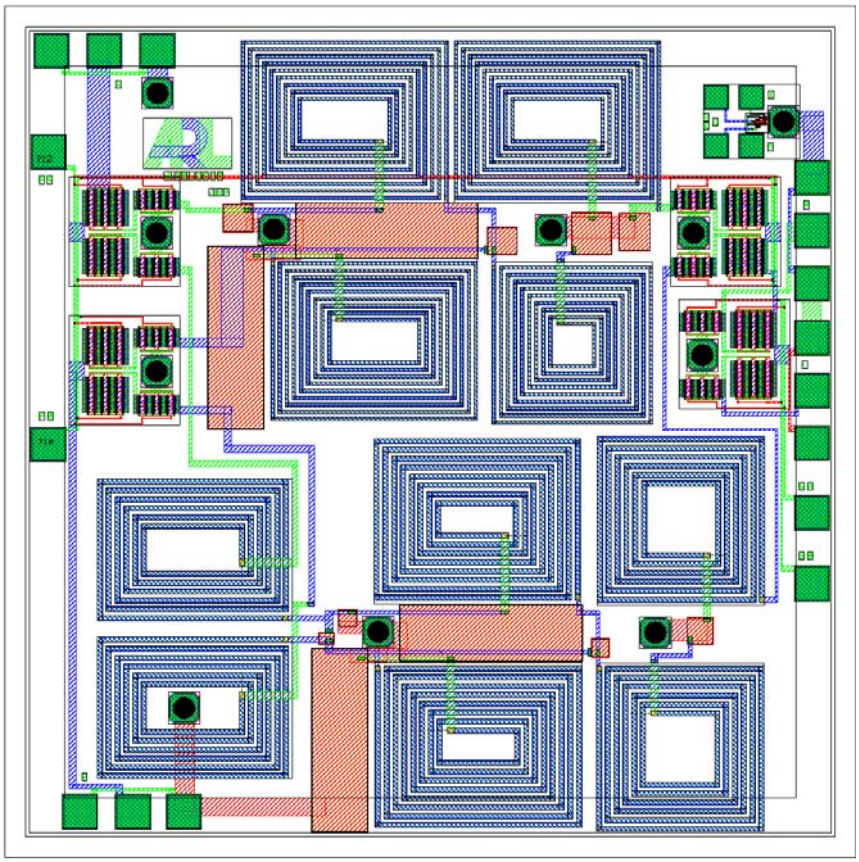

Figure 78. Layout of ARL26DB (2.41x2.41 mm die).

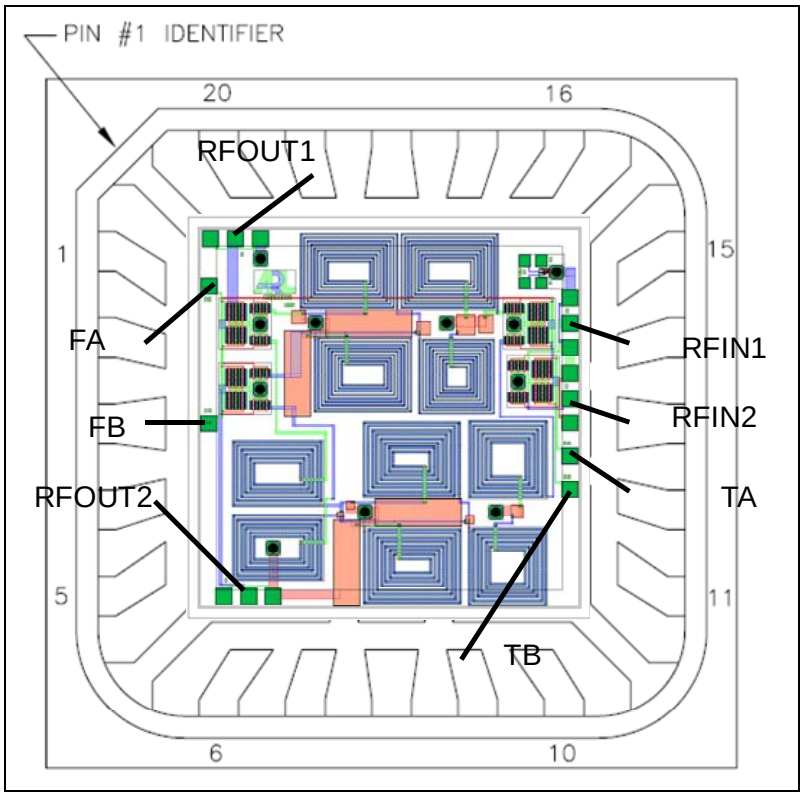

Figure 79. Wire-bond diagram of ARL26DB in a 4x4 mm QFN package.

The circuit designated as ARL27M425 is designed for matching the CC1000 at 425 MHz (figure 80). The values of the lumped elements in the matching circuits are those recommended in the CC1000 data sheet. However, the topology is split into an RF input and an RF output. The CC1000 has two single ended RF connections, one intended for input and one intended for output with an internal TR switch whose effect on the impedance is not specified in the data sheets. Originally, the topology connects a shunt inductor/series capacitor matching element to each of the CC1000 RF connections, which then connect to a simple low pass filter leading to a single RF antenna connection. Since the booster IC has a separate transmit path and receive path, the topology of this design uses two separate paths with two separate low pass filters, each connected to a series inductor/shunt capacitor combination for matching. In the layout, the upper-left connects to the booster low noise amplifier/receive path and the lower-left connects to the CC1000 RF input. Likewise, the upper right connects to the Booster power amplifier/transmit path and the lower right connects to the CC1000 RF output. A preliminary wire-bond diagram of the die in a 4x4 mm, SEMPAC, 20-pin, 4x4 mm QFN package is shown in figure 81. Note that this circuit is entirely passive, i.e., uses only lumped elements.

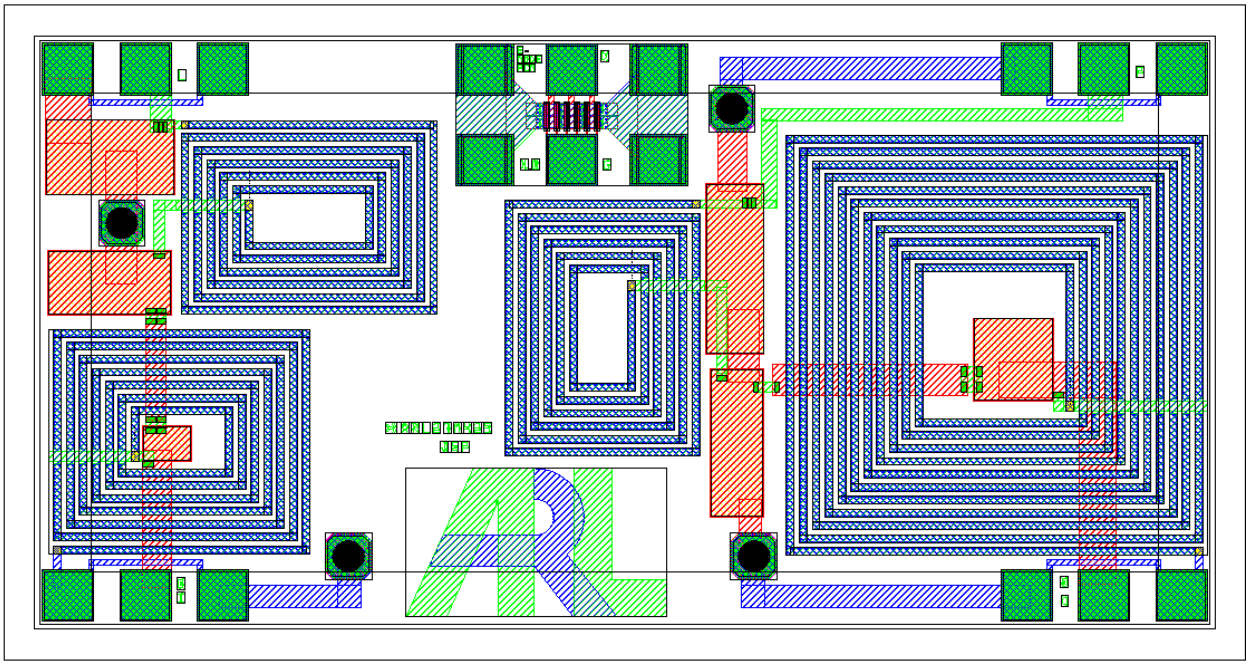

Figure 80. Layout of ARL27M425 (2.41x1.27 mm die).

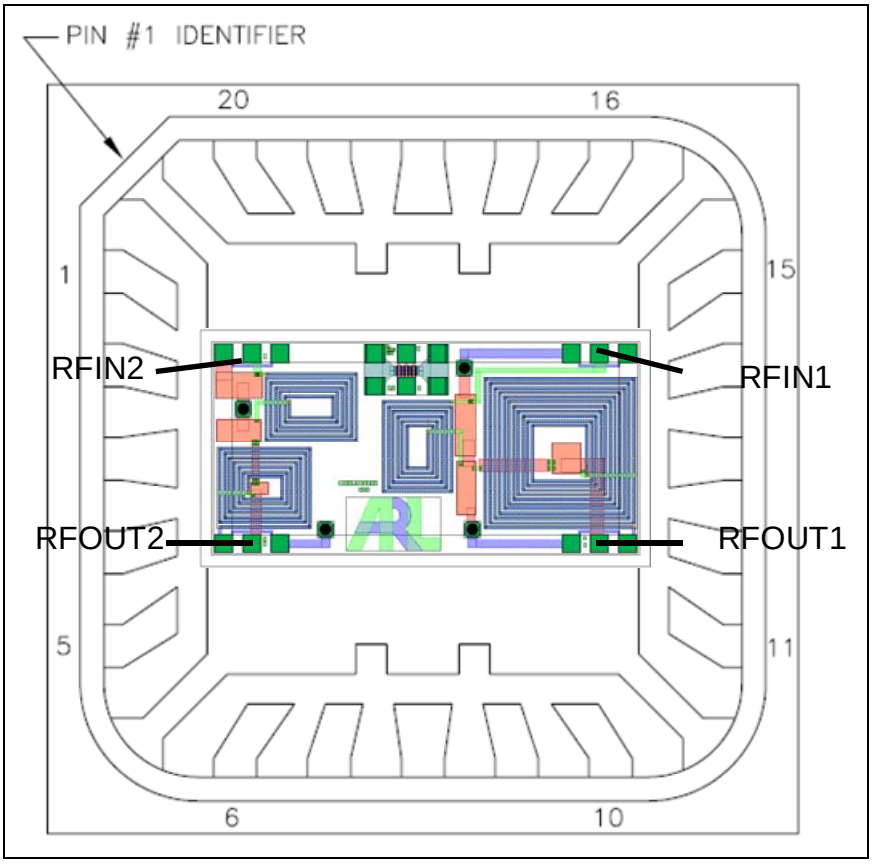

Figure 81. Wire-bond diagram of ARL27M425 in a 4x4 mm QFN package.

The circuit designated as ARL28M900 is designed for matching the CC1000 at 900 MHz (figure 82). The values of the lumped elements in the matching circuits are those recommended in the CC1000 data sheet. This circuit's topology is exactly the same as that described for ARL27M425, the difference is the change of lumped element values to suit the higher frequency band. In the layout, the upper left connects to the booster low noise amplifier/receive path and the lower left connects to the CC1000 RF input. Likewise, the upper right connects to the booster power amplifier/transmit path and the lower right connects to the CC1000 RF output. A preliminary wire bond diagram of the die in a 4x4 mm SEMPAC, 20-pin, 4x4 mm QFN package is shown in figure 83. Note that this circuit too is entirely passive, i.e., uses only lumped elements.

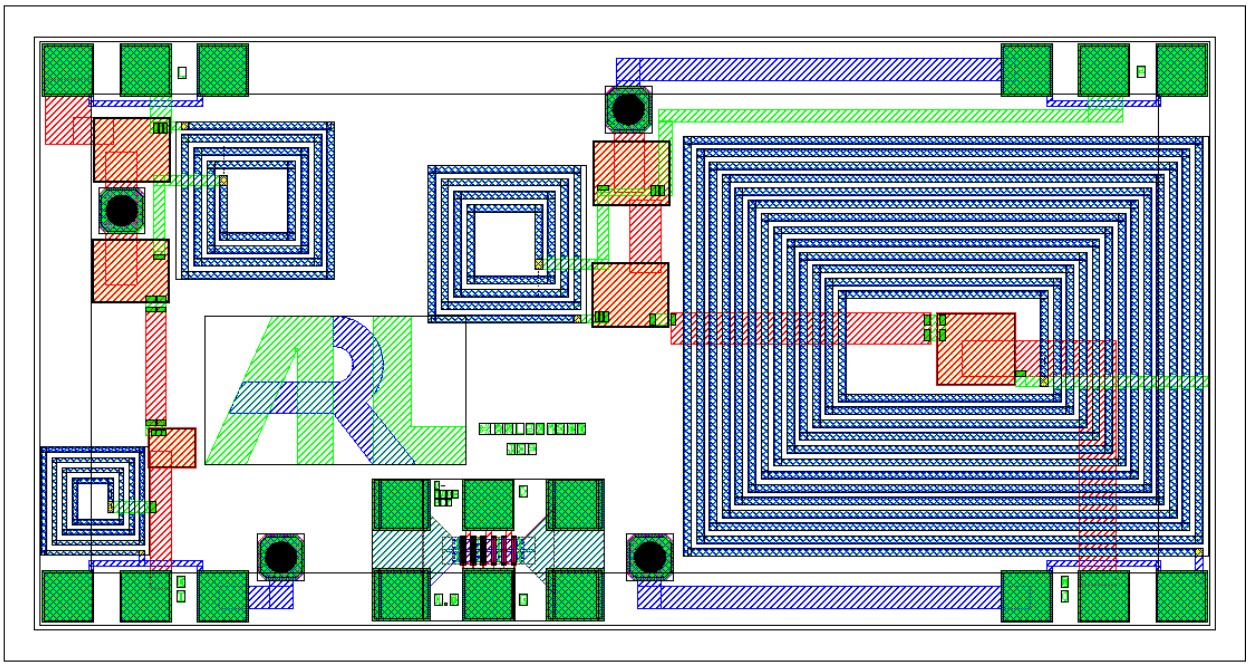

Figure 82. Layout of ARL28M900 (2.41x1.27 mm die).

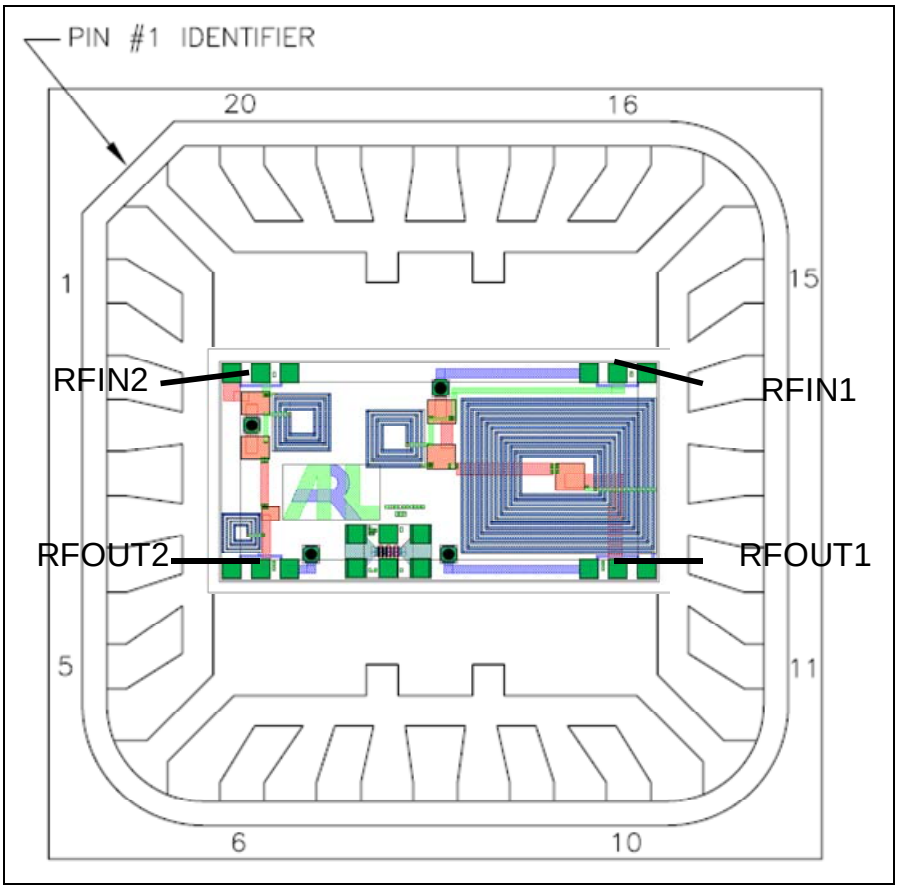

Figure 83. Wire-bond diagram of ARL28M900 in a 4x4 mm QFN package.

The circuit designated as ARL29M425 is designed for matching the CC1100 at 425 MHz (figure 84). The values of the lumped elements and the topologies of the matching circuits are those recommended in the CC1100 data sheet. In the layout, connections to the CC1100 are on the upper-left and lower-left sides of the layout creating a differential RF connection while the right-hand side of the layout is a single-ended RF connection, intended to be the antenna. This circuit will demonstrate the improved SWAP by integrating the matching elements for the CC1100. However, this design has a single RF connection, while the booster IC has a separate single ended RF connection for the transmit and receive paths—see ARL29M425S. A preliminary wire-bond diagram of the die in a 4x4 mm SEMPAC, 20-pin, 4x4 mm QFN package is shown in figure 85. Note that this circuit is entirely passive, i.e., uses only lumped elements.

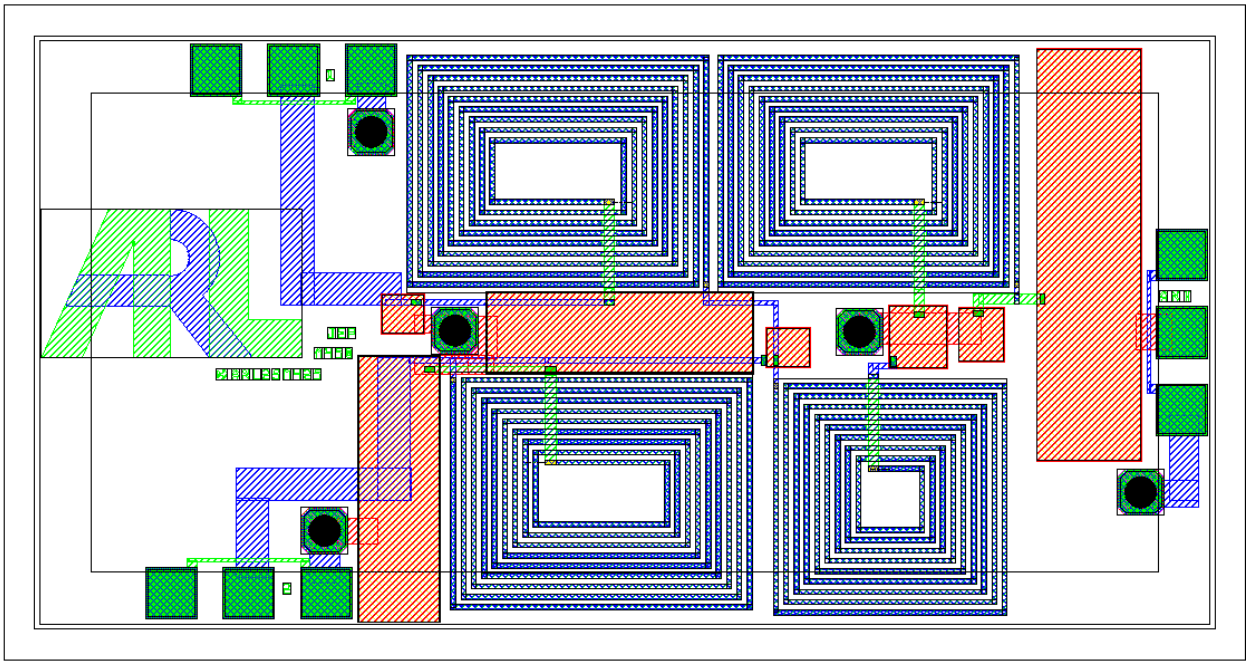

Figure 84. Layout of ARL29M425 (2.41x1.27 mm die).

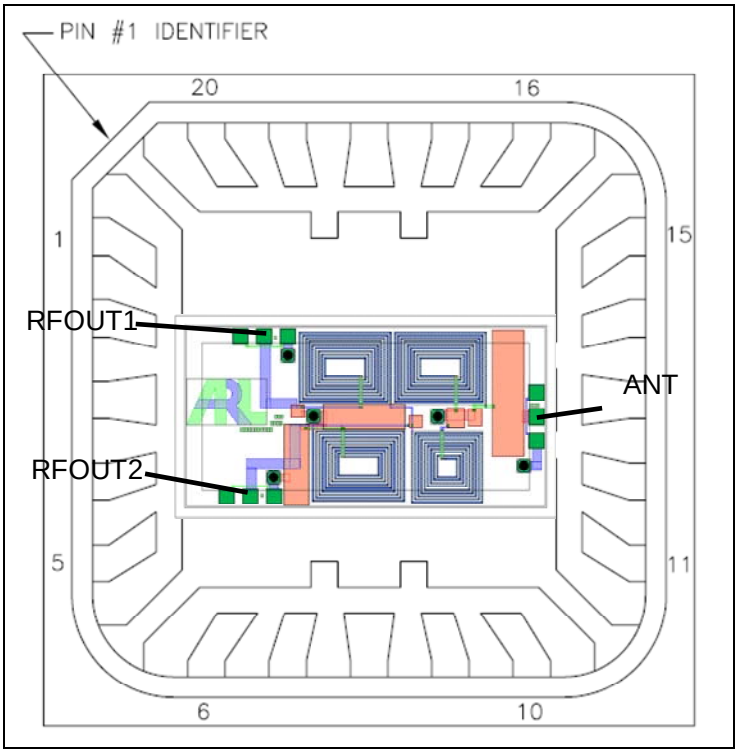

Figure 85. Wire-bond diagram of ARL29M425 in a 4x4 mm QFN package.

The circuit designated as ARL29M425S is designed for matching the CC1100 at 425 MHz (figure 86) and is based on the ARL29M425 design. The difference between the designs is the addition of a single pole double throw TR switch to connect the single-ended “antenna”

connection to either the transmit or receive RF connections of the booster IC. In the layout, the differential RF connection to the CC1100 is on the upper-left and lower-left sides while the right-hand side has a TR switch to connect to either a singled-ended RF connection to the right or to the bottom. A preliminary wire bond diagram of the die in a 4x4 mm SEMPAC, 20-pin, 4x4 mm QFN package is shown in figure 87. Note that this circuit is mostly passive, i.e., uses lumped matching elements, but also uses PHEMTs as switches to choose between one of two single ended RF connections.

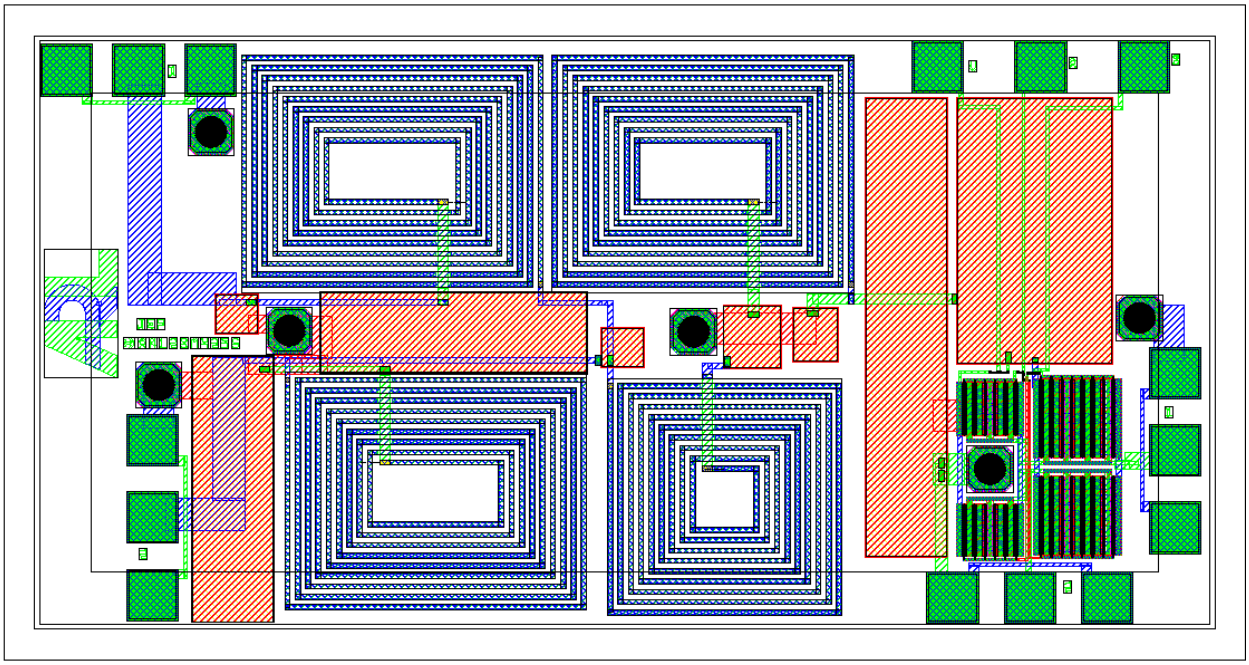

Figure 86. Layout of ARL29M425S (2.41x1.27 mm die).

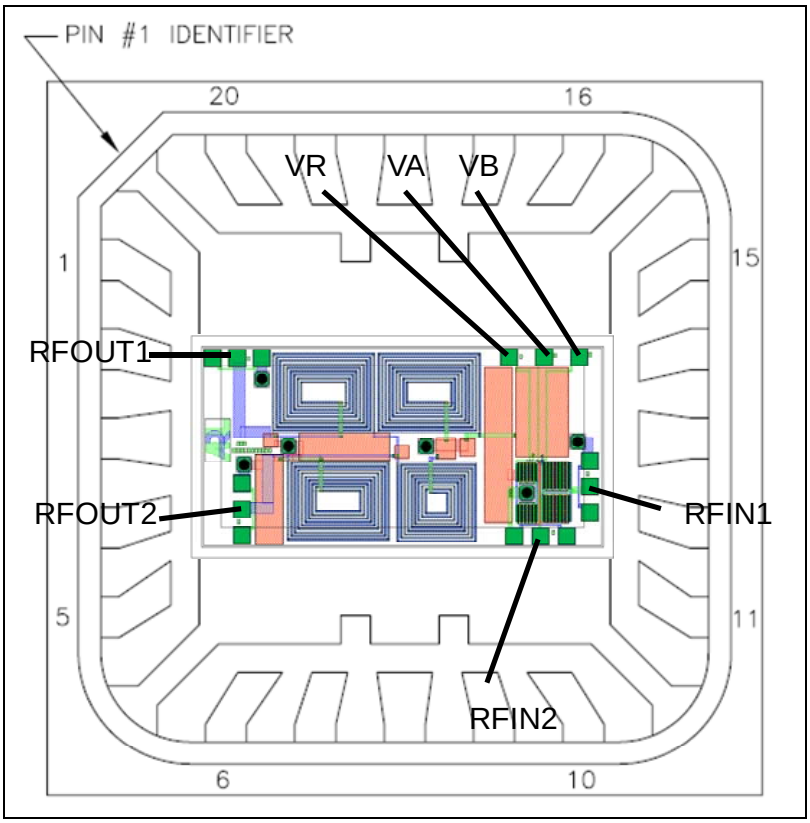

Figure 87. Wire-bond diagram of ARL29M425S in a 4x4 mm QFN package.

The CC1110 data sheet gives the differential port impedance towards the antenna as 116 + j41 Ω at 433 MHz, and 86.5 + j43 Ω at 868 MHz. For the CC1000, the singled-ended receive mode impedance is at 70 + j26 Ω 433 MHz and 52 + j4 Ω at 915 MHz, while the singled-ended transmit mode impedance is at 140 Ω 433 MHz and 80 Ω at 868 MHz. Simulations of recommended matching circuits for both the CC1100 and CC1000 resulted in slightly different answers for both sets of circuits. Also, the simulations for the CC1000 seemed to be very narrowly resonant circuits that were not near the 50-ohm match point of the Smith chart. At least the CC1100 matching circuit simulations seemed to have a wider resonance and were closer to the 50-ohm match point of the Smith chart. At these relatively low frequencies, the lumped element parasitics should be fairly small. A design kit of the suggested 0402 Murata chip capacitor and chip inductor elements was obtained for Agilent's ADS program, and the matching circuits were re-simulated with results similar to using ideal elements. There were no boards for either the CC1000 or CC1100 RFICs to measure and verify the discrepancies in the data sheets. So, it is likely that these matching circuit designs will not be ideal for this 1st pass of designs. From the simulations, it would appear that the CC1100 circuits are more likely to be "close" to the desired impedance match. At least, the matching circuits should demonstrate the system SWAP improvement and feasibility of integrating the many lumped element matching elements required by a typical RFIC transceiver into a single compact IC. Also, it should be noted that the data sheet for the CC1000 has a component designated as C41, which TI recommends omitting

for the CC1000 UltraCSP package. But that omission may be the cause of some problems seen in a tag design by Sandia. Their experience seems to indicate that the system works better if you include C41, an indication that impedance matching for the CC1000 may be critical and very sensitive, in addition to verifying an error in the data sheet.

The schematic for the CC1100 matching circuit at 433 MHz is shown in figure 88 and for 900 MHz in figure 89. Note that they are similar but slightly different topologies. It would be good to explore the possibility of creating a single broadband topology of lumped elements that could create the desired match for both bands without having to use the switched topology approach used in the ARL26DB design. Simulations showing similar agreement between the TriQuint element matching circuit and the original ideal element match are shown in figure 90 for the 433-MHz design and figure 91 for the 900-MHz design. A layout was created for the 900-MHz matching circuit but it was not included in this tile for fabrication, only the 433-MHz design was created as ARL29M425 with a single RF connection to an antenna, and as ARL29M425S, which includes a TR switch to connect to the transmit and receive RF connections of the booster IC.

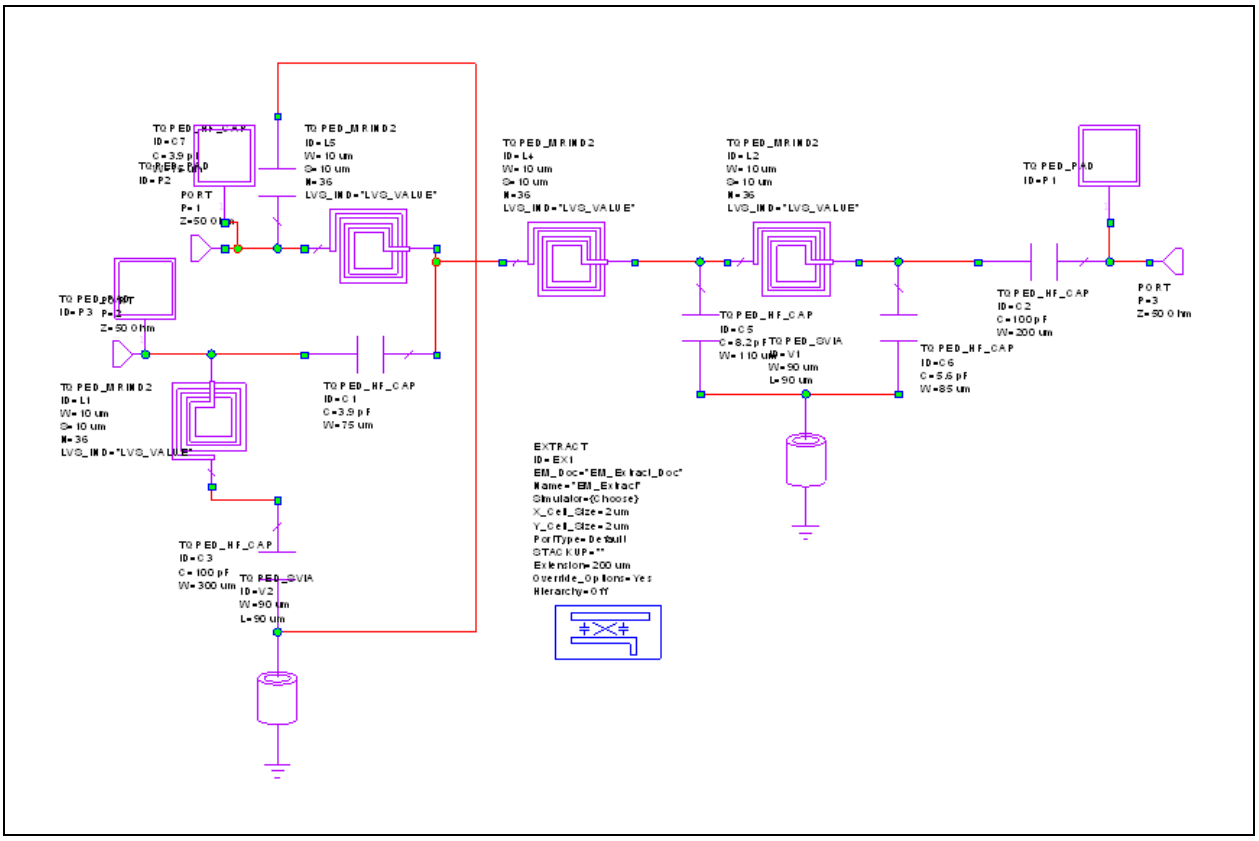

Figure 88. Schematic of the CC1100 matching circuit for 425/433 MHz using TriQuint elements.

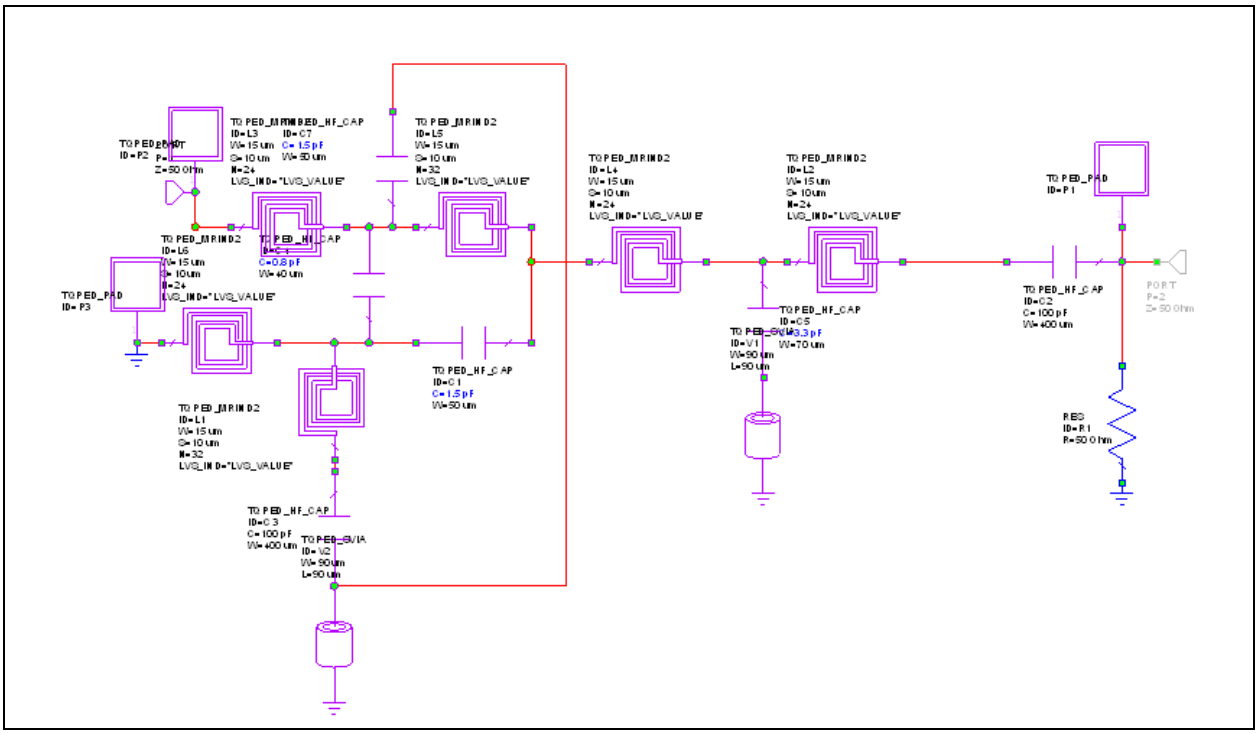

Figure 89. Schematic of the CC1100 matching circuit for 900 MHz using TriQuint elements.

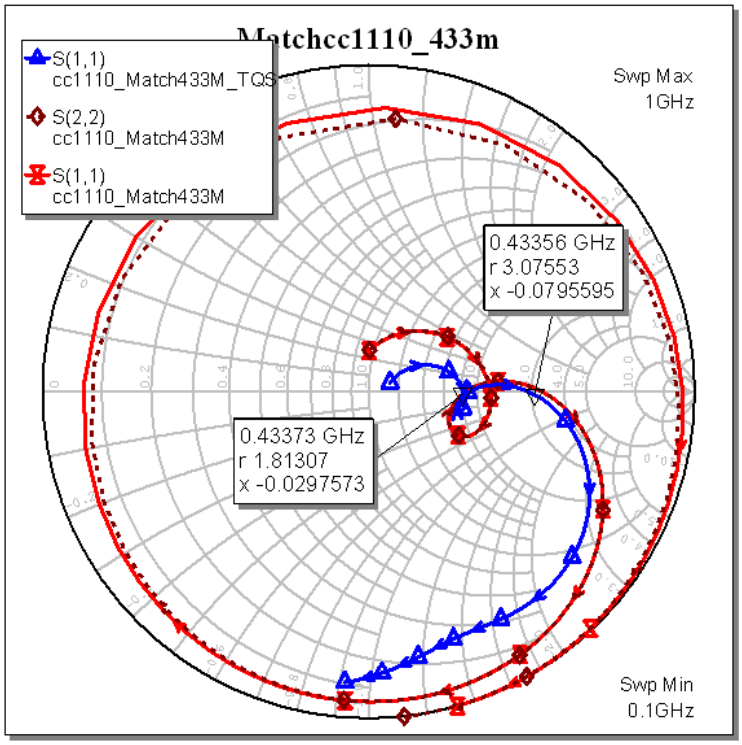

Figure 90. Simulation of the CC1100 matching circuit for 425/433 MHz (TQS and ideal).

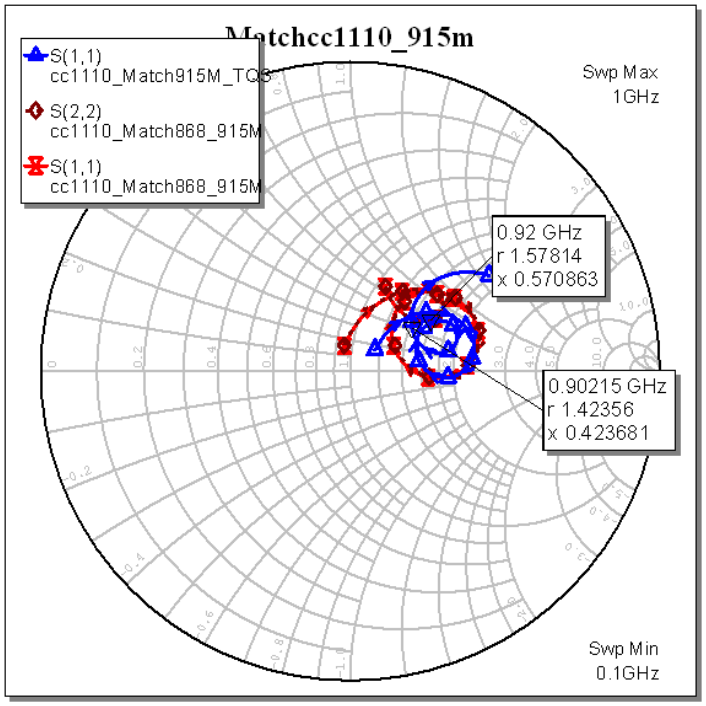

Figure 91. Simulation of the CC1100 matching circuit for 900 MHz (TQS and ideal).

The schematic for the CC1000 matching circuit at 433 MHz is shown in figure 92 and for 900 MHz in figure 93. Note that they are identical except for the capacitor (C41), which is recommended for the lower frequency bands if the UltraCSP package is not used. It would be good to explore a single broadband topology of lumped elements that could create the desired match for both bands, but it looks like it would be very difficult for this part based on these simulations. Also, the topology of the matching circuit assumes a single RF connection to an antenna. For use with the booster IC, the matching circuits were split into a separate transmit and receive path as shown in figure 94. Figure 95 shows a Smith chart simulation of the RF input and RF output impedances for the recommended matching circuits of the CC1000 at 315, 433, and 868 MHz. It is a cluttered plot, but what is evident is that each band seems to have a narrow resonance that is not as close to the 50-ohm Smith chart center as one would want. Also the simulated impedances do not match the recommended values, and there is the possibility that the internal TR switch of the CC1000 has some effect on the impedances that is not documented. For simulation purposes, the matching circuits were split into a low pass filter and two series capacitor/shunt inductor matching elements for the RF input and output. Then these sub circuits using TriQuint elements were tuned to match the corresponding ideal element versions, shown in the simulations at 433 MHz (figure 96). The only dual band matching design was for the newer CC1100 RFIC parts. Figure 97 shows the schematic of ARL26DB where a set of three switches

select either the matching circuits at 433 or 900 MHz followed by a switch to select either the transmit or receive RF connection of the booster IC.

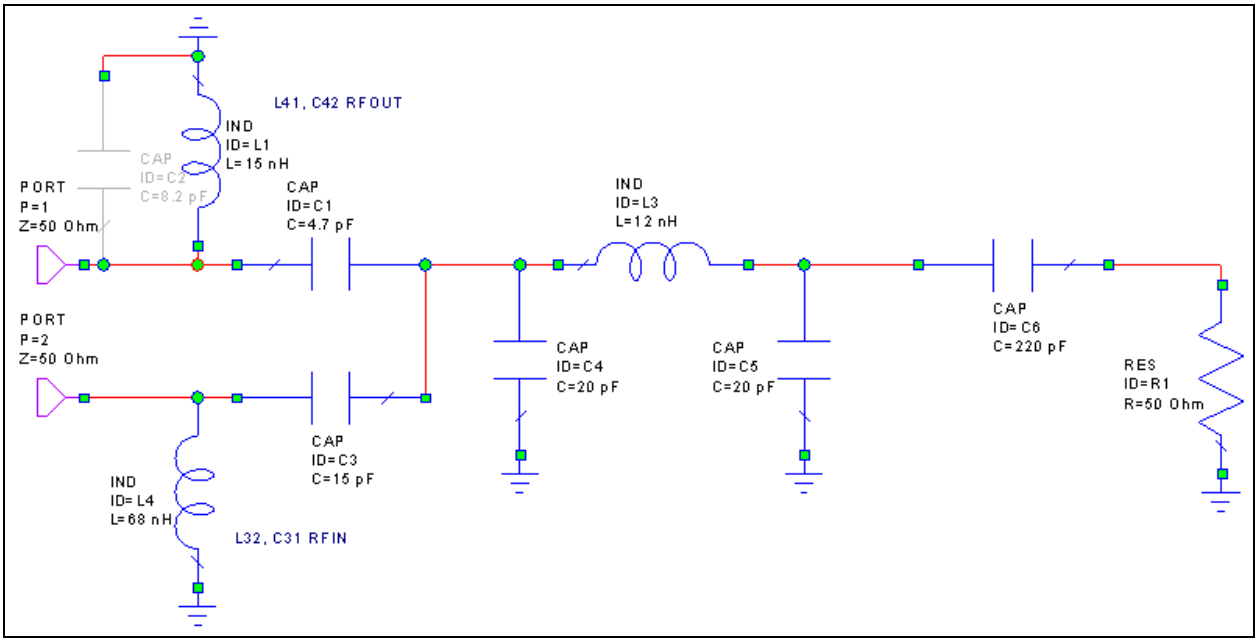

Figure 92. Schematic of the CC1000 matching circuit for 433 MHz using ideal elements.

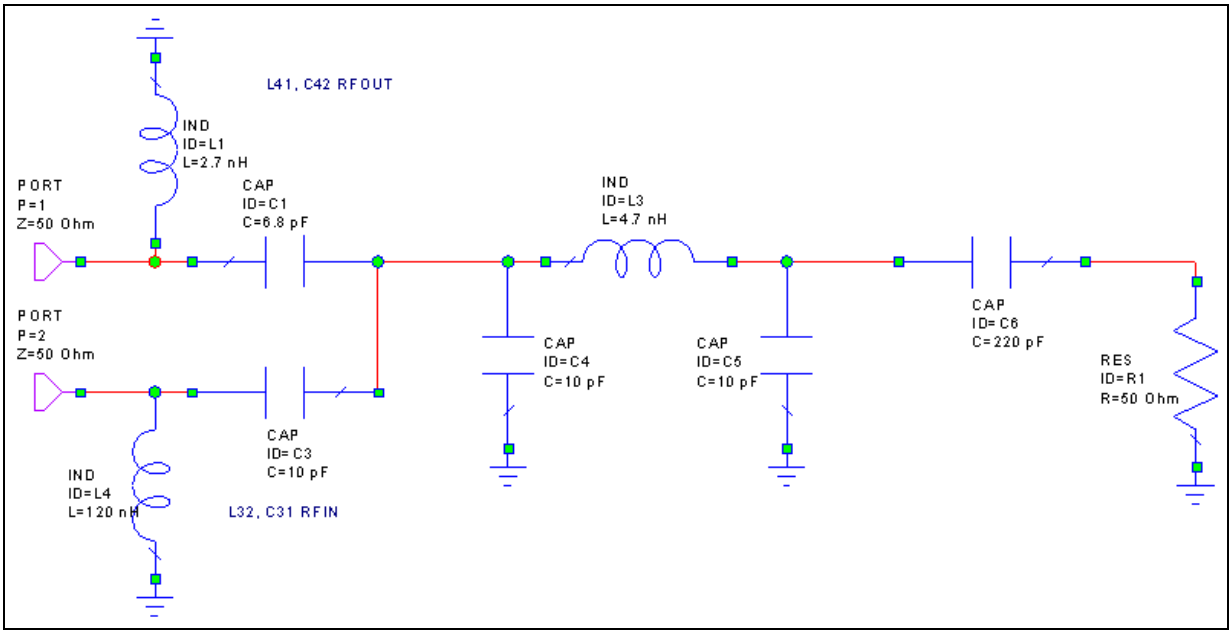

Figure 93. Schematic of the CC1000 matching circuit for 900 MHz using ideal elements.

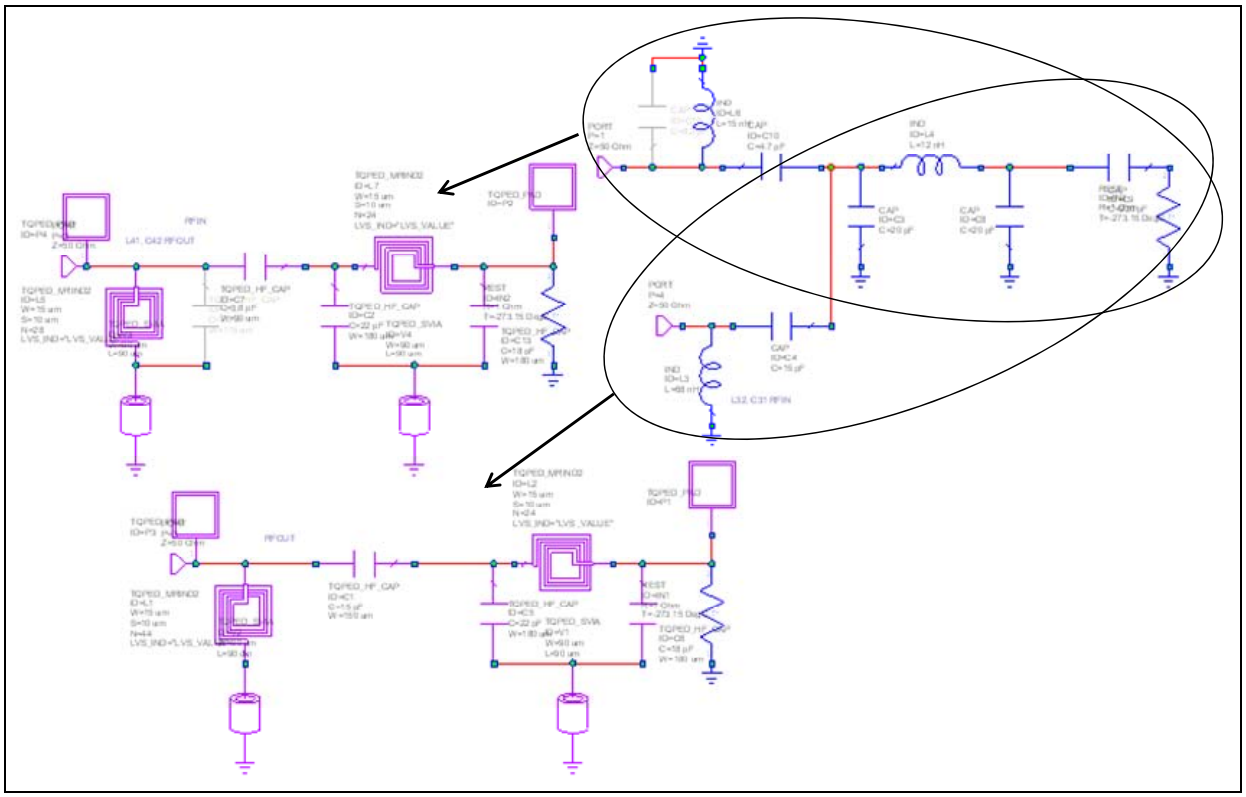

Figure 94. Split of the CC1000 matching circuit into separate transmit and receive circuits.

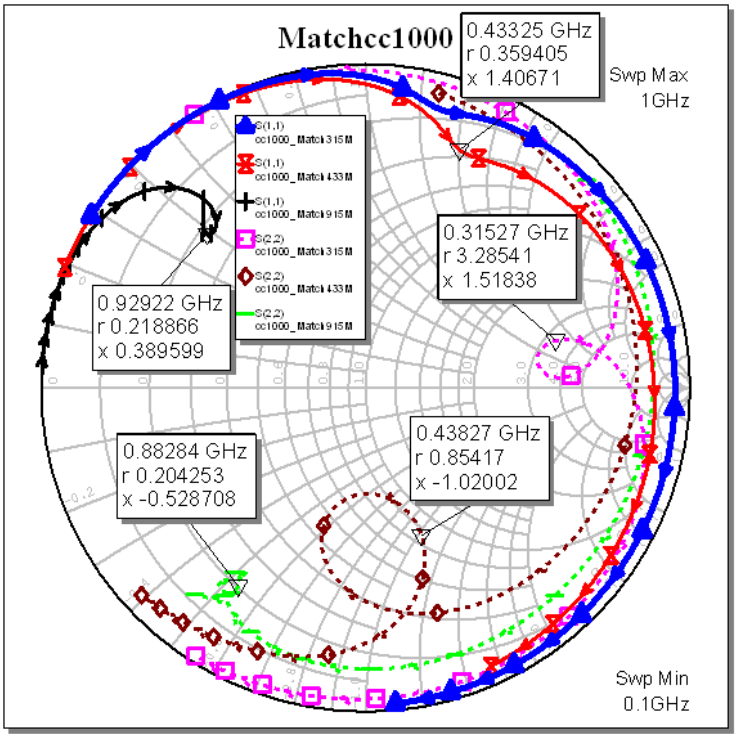

Figure 95. Simulation of the CC1000 matching circuits for 315, 433, and 900 MHz (ideal).

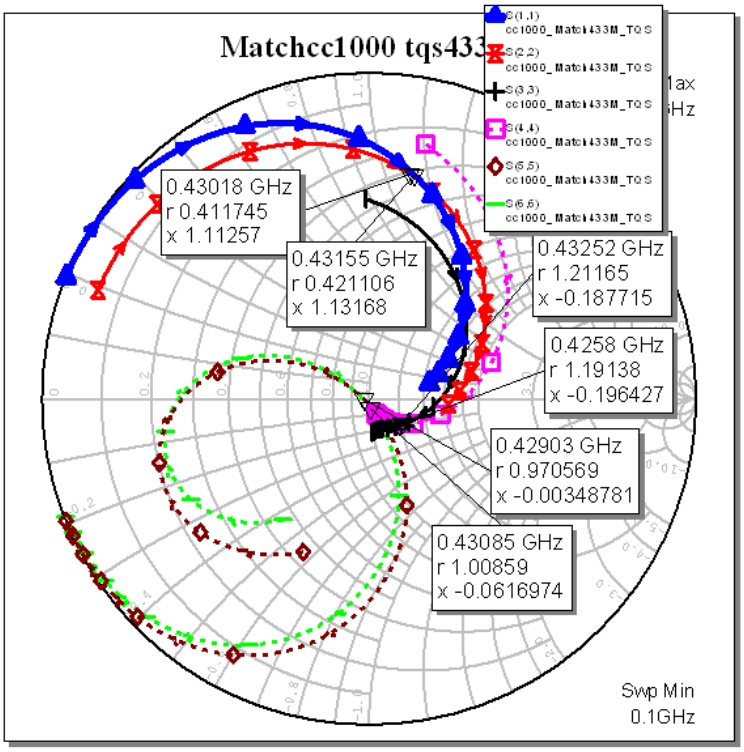

Figure 96. Simulation of the CC1000 split matching circuits for 433 MHz (TQS and ideal).

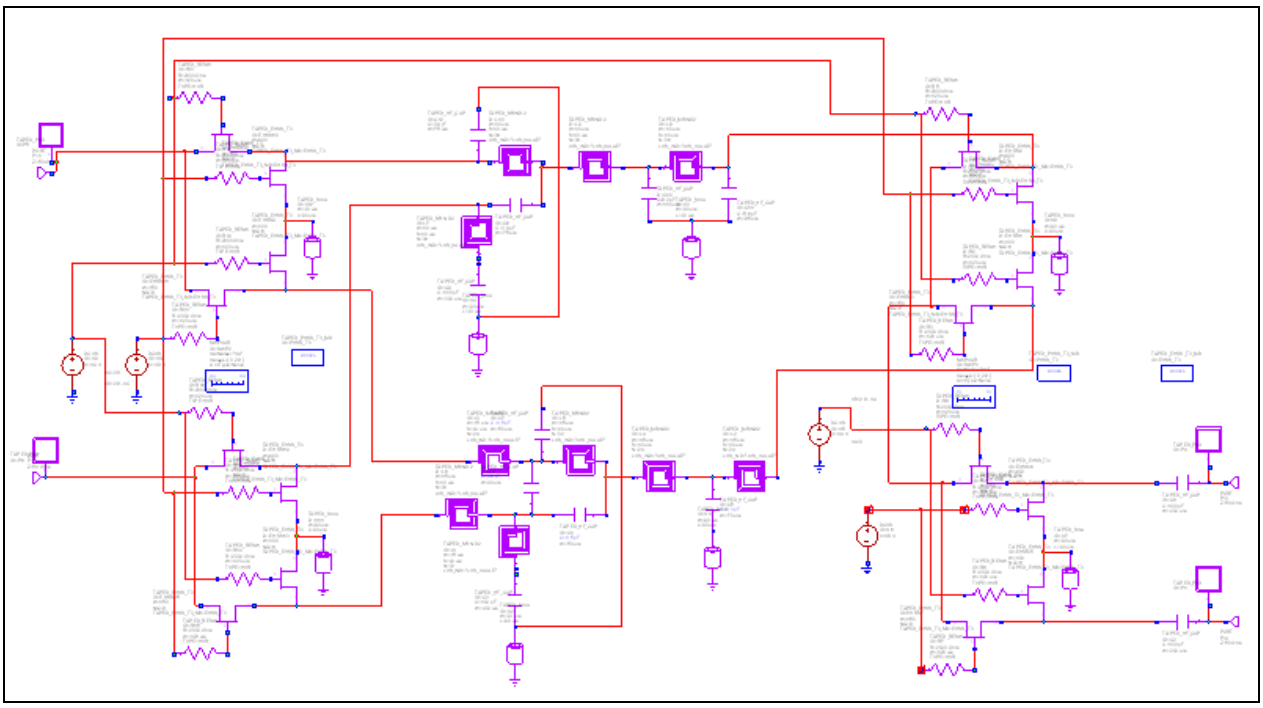

Figure 97. Schematic of the CC1100 dual band matching circuit (ARL26DB).

6. Design Rule Checking (DRC)

All designs within the tile must be checked according to the process design rules supplied by TriQuint. TriQuint has design rules for their fabrication processes that work with the open-source ICED program. Design verification typically consists of design rule checking (DRC) and layout versus schematic checking (LVS). For fabrication feasibility, TriQuint only cares that the tile passes DRC checks and can be fabricated. While some design rules may be oriented towards maximizing yield and are not fatal errors, any violations of the design rules must be removed or granted a waiver to fabricate by the foundry. Additionally, it is up to the designer to verify that the designs are connected as desired and that parameter values are correct by doing additional LVS checking. After completing DRCs with ICED, a final DRC check was performed on the tile layout using TriQuint's "mailDRC" service. TriQuint provides a free e-mail based service to provide a final DRC check using Cadence's Assura software. Next, there is a checklist for the foundry to verify higher level fabrication issues such as labeling. Each individual die must have a unique label using the correct metal layer and be of sufficient size. Every die name starts with the letters "ARL" to help identify the customer so that the individual dice can be sorted and returned appropriately. The second ARL tile passed the mailDRC checking by TriQuint and was accepted for integration into the fabrication process.

7. Layout versus Schematic (LVS) Checking

Each design is verified against a schematic (i.e., a netlist), which can be generated from MWO or ADS. Both tools require manual editing of the generated netlist, which typically requires an iterative LVS check until all device connections are verified. Foundries do not require LVS checking, only DRC checking, but it is imperative for the designer to verify the connections in the layout. A DRC correct layout does not guarantee that there are no shorts or opens that could cause the circuit to fail. Verifying the connections requires LVS checking followed by a final DRC check if any layout changes occur. If the design passes DRC and LVS checking, then the probability of functional success is extremely high. In addition to checking the connections, the LVS check also notes parametric differences between the schematic and layout. If the capacitors, resistors, or PHEMTs differ in size, type, or value, the LVS check will list the mismatches. Inductors are not checked parametrically, only their connectivity is verified. All of the designs on the second ARL tile passed LVS checking. The LVS checks did find at least one major error in connectivity that was not found by DRC checks alone.

Another check beyond DRC and LVS checks are electrical rules. It is a good idea to check the high current paths in every design—i.e., the active designs for this tile. The path for drain current to the PHEMTs in the power amplifiers is the most likely area for concern. A minor increase in a line width for the drain connection to the 50-mW, 425-MHz power amplifier was performed after examining the designs.

8. Tile Layout

The prototype fabrication offered by TriQuint provides a 5x10 mm quarter tile, which the designer can partition into multiple designs. There are a number of limitations, for example, all the rows and columns must align. Typically the row and column dimensions are limited to a few choices and may even use multiples of some fixed value. Since these designs were targeted for a 4x4 mm QFN package, the 95-mil dimension was chosen to provide the maximum circuit design area. Die size versus the number of different designs is a tradeoff in the tile layout. For the smaller matching circuits, the width was made 95 mils to fit in the 4x4 mm QFN package, but the height was reduced to 50 mils to yield an extra row of designs (two). Half of the 10 designs in the tile are active booster IC designs and half are dedicated to integrating the RFIC matching circuits into a single IC to improve SWAP. Figure 98 shows a plot of the final 4.82x9.77 mm ARLTILE2. Table 19 lists the design locations within the tile. Each design will get diced into individual gel packs with typically 50 copies of each of the 10 designs for test.

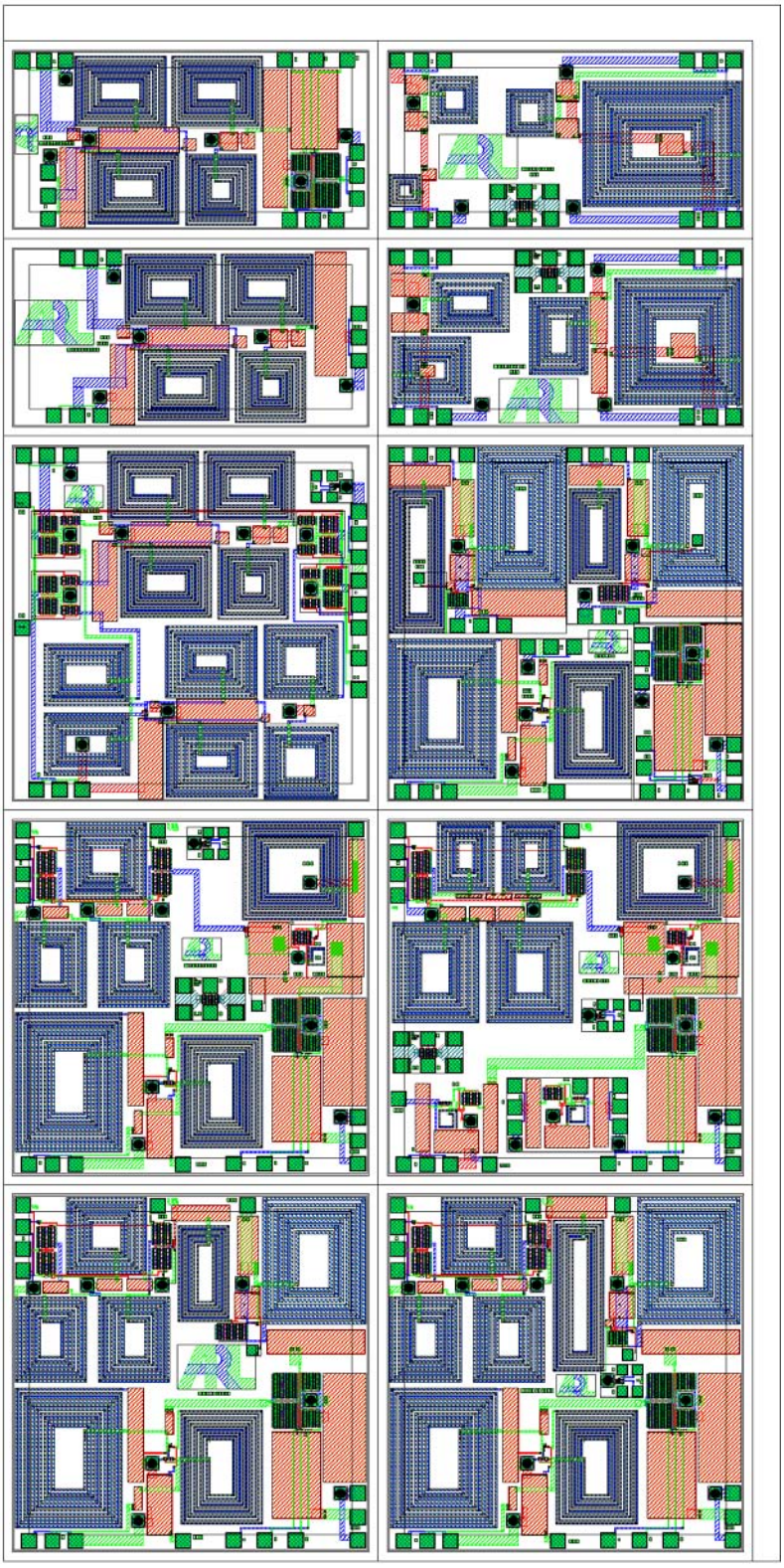

Figure 98. Layout plot of ARLTILE2 (10 designs–4.8x9.8 mm)

Table 19. Map of design layout within ARLTILE2.

Die Size (Y µm)	Row	2410 X µm	
		C1	C2
1270	R1	ARL29M425S	ARL28M900
1270	R2	ARL29M425	ARL27M425
2410	R3	ARL26DB	ARL25
2410	R4	ARL23M425	ARL24DB
2410	R5	ARL21M425	ARL22M425

The designs were submitted August 24, 2010, to TriQuint for fabrication. It is expected that they will be returned in late October 2010 when probe testing of the individual die will be performed. Designs will also be packaged for testing the die plus package. The goal is to integrate the most promising designs into a wireless system to demonstrate the enhanced performance and improved SWAP of the booster IC and integrated matching circuit designs.

9. Conclusion

While I performed the designs, the end product was a team effort. A design review held with many participants, mostly in the RDRL-SER-E branch, was very helpful in making sure that these were the best designs achievable under the existing constraints. A number of people helped with the testing, reviewing, and documenting of the 1st pass booster IC designs, which were then used as a basis for these optimized 2nd pass designs. For further documentation of the 1st pass designs and TriQuint design package for the 2nd pass, see the references 1–5.

10. References

1. Mitchell, G.; Penn, J. *Preliminary Gallium Arsenide (GaAs) Integrated Circuit Design for Radio Frequency Booster Chips at 450, 900, and 2400 MHz*; ARL-TR-4970; U.S. Army Research Laboratory: Adelphi, MD, September 2009.

2. Penn, J. GaAs *Microwave Integrated Circuit Designs Submitted to TriQuint Semiconductor for Fabrication*; ARL-TN-0381; U.S. Army Research Laboratory: Adelphi, MD, December 2009.

3. Mitchell, G.; Penn, J. *Results of Bare Die Probing for RF Booster Chip at 400, 900, 2400 MHz*; ARL-TR-5170; U.S. Army Research Laboratory: Adelphi, MD, April 2010.

4. Penn, J. *Testing of GaAs Microwave Integrated Circuit Designs in QFN Packages*; ARL-TR-5131; U.S. Army Research Laboratory: Adelphi, MD, March 2010

5. Penn, J. *GaAs Microwave Integrated Circuit Designs Submitted to TriQuint Semiconductor for Fabrication (ARL Tile #2)*; ARL-TN-0404; U.S. Army Research Laboratory: Adelphi, MD, September 2010.

List of Symbols, Abbreviations, and Acronyms

ADS	Advanced Design System
AWR	Applied Wave Research
BPSK	binary phase shift keying
CAD	computer-aided design
DMODE	depletion mode
DRC	design rule checking
EM	electromagnetic
EMODE	enhancement mode
GaAs	gallium arsenide
IC	integrated circuit
ICED	Integrated Circuit Editor
LVS	layout versus schematic checking
MMIC	monolithic microwave integrated circuit
MWO	Microwave Office
PAE	power added efficiency
PHEMT	pseudomorphic high electron mobility transistor
QFN	quad flat no lead
RF	radio frequency
RFIC	RF integrated circuit
TI	Texas Instruments
TR	transmit/receive
UHF	ultra-high frequency

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